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# FX003

# QTC Selective Call Tone Decoders

**Obsolete Product**
**- For Information Only -**

**Publication D/003/4 February 1990**

- **15-Tone Selcall Decoder**
- **Group Call and Data Capability**
- **Excellent Noise Performance**
- **4 Bit Data Output**
- **Few External Components**
- **CCIR, ZVEI, EEA, EIA Tone Sets**
- **$\mu$ Processor Compatible**
- **High Dynamic Range**
- **Low Power CMOS**
- **On-Chip Oscillator Uses Low-Cost Resonator**

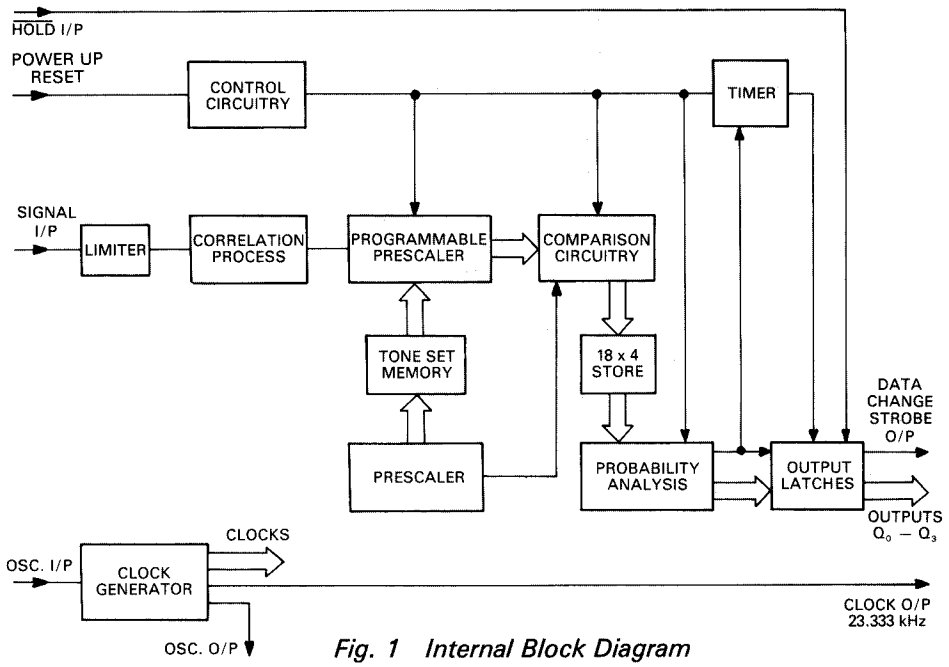



*Fig. 1 Internal Block Diagram*

**FX003QC**
**FX003QZ**
**FX003QE**
**FX003QA**
**FX003QZS**

The FX003 is a CMOS QTC (Quadradecimal Tone Coding) tone decoder which may be used to decode Selcall tones in accordance with CCIR, ZVEI, EEA and EIA international tone standards.
The FX003 detects an input frequency falling within any of the fifteen tone channels programmed on-chip and outputs the hexadecimal tone number in 4-bit binary code. When a tone is detected, its 4-bit code is latched at the data outputs and a Data Change is generated. Failure to qualify any tone for a continuous period of 33 ms causes the output to be set to 'Notone' (16th logic state) and a Data Change strobe to be generated.
A DATA CHANGE output signals each change in the output code and can be used with the HOLD/ACKNOWLEDGE input to establish handshake routines with microprocessors and other data processing logic.
A 'Power Up Reset' (PURS) routine ensures all internal circuitry is correctly reset when power is first applied to the device. Following 'PURS' the FX003 generates HEX 'E' (NO DATA CHANGE) which in turn is followed by a normal decode sequence.
The on-chip inverter may be used with a resonator to provide the 560 kHz master clock for the device, or an external clock may be used. A divided down buffered 23.33 kHz clock output is also provided for use with other '03 devices and trimming of the 560 kHz resonator.
The FX003 is available in a number of pin compatible versions, each version programmed in accordance with the frequencies and bandwidths of a specified QTC toneset.

| Pin Description *(See Figure 2)* | | | Function |
|---|---|---|---|
| D.I.L. FX003* | Chip Carrier FX102K *(see Note A)* | Chip Carrier FX202*K *(see Note A)* | *QC, QZ, QE, QA, QZS |
| 1 | 2 | — | **23.333 kHz Clock O/P:** A 23.333 kHz buffered squarewave logic output directly derived from the oscillator frequency (nominally 560.0 kHz). May be used for auxiliary functions e.g. 560 kHz resonator trimming,external timing of received tone periods and for other '03 family products. |
| 2 | 4 | — | **$\overline{\text{Xtal}}$:** Output from on-chip inverter. |
| 3 | 6 | — | **Xtal/Clock:** Input to on-chip inverter may be used in conjunction with $\overline{\text{Xtal}}$ O/P and 560 kHz resonator or as a buffered input for an external clock (nominally 560.0 kHz). |
| 4 | 10 | 5 | **VSS:** Negative supply. |
| 5 | — | 8 | **$\overline{\text{Hold}}$ I/P:** Active when at VSS. If hold is taken to VSS when the input tone changes it latches the next data change pulse at logic 1 until the $\overline{\text{Hold}}$ is returned to VDD. This facilitates Interrupt/Handshake routines for micro-processors when used in conjunction with the Data Change O/P. Tie to VDD if not used. |
| 6 | — | 9 | **Power Up Reset:** A logic 1 level of at least 1 ms duration is required at this pin to reset internal circuitry on power-up. For slow-rising power supplies increase the time constant of the components shown accordingly. |
| 7 & 16 | 1 3 5 7 8 9 11 12 14 15 16 18 20 21 22 23 25 27 | 1 2 3 6 7 10 11 13 14 15 18 20 23 24 26 28 | **Internally Connected/Open Circuit:** Should be left open circuit. |
| 8 | — | 16 | **Data Change:** A pulse is generated at this pin shortly after detection of a tone and new data being presented at the $Q_0$ — $Q_3$ outputs *(see Figure 5 Timing Diagram).* |
| 9 | — | 22 | $Q_3$ **Data Outputs:** A 4-bit word which |
| 10 | | | $Q_2$ is output after a successful decode |
| 11 | | | $Q_1$ and represents the Hex code for the |
| 12 | | | $Q_0$ decoded tone frequency. |
| 13 | 19 | 25 | **VDD:** Positive Supply. |
| 14 | 24 | — | **Signal Input:** Audio selcall tones are a.c. coupled to this pin via a capacitor. D.C. bias of the internal high gain limiter is set up by connecting this pin via a resistor to the bias pin. |
| 15 | 26 | — | **Signal Bias:** These pins should not be loaded with any other circuitry. |
| — | — | 3 | 93.333 kHz Osc I/P — FX102K/FX202*K: Interchip connections. |
| — | 13 | — | 93.333 kHz Osc O/P. — These pins should not be loaded with any external |
| — | — | 27 | Logic Signal I/P. — circuitry. |
| — | 17 | — | Logic Signal O/P — FX003*D.I.L: internally connected. |

**Note A:**
*FX102K and FX202*K are sold as a pair, and represent the same circuit function as the FX003* D.I.L. device.*

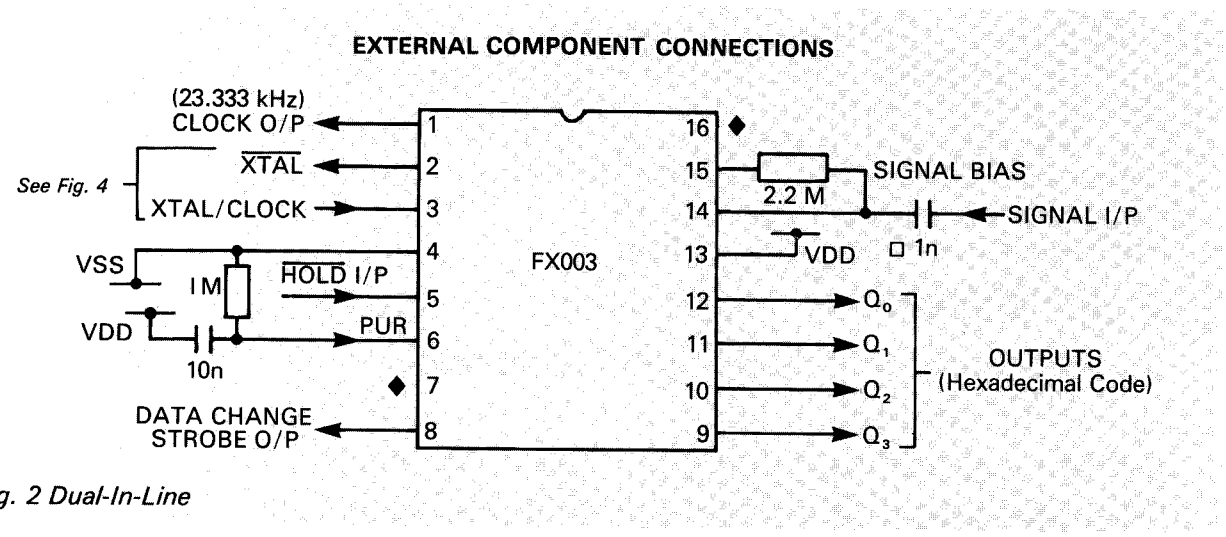



*Fig. 2 Dual-In-Line*

* *QC, QZ, QE, QA, QZS*
◆ *No connection. Do not tie.*
□ *1n recommended value for C, Z, E and ZS versions.*
*2.2n recommended value for the A version.*

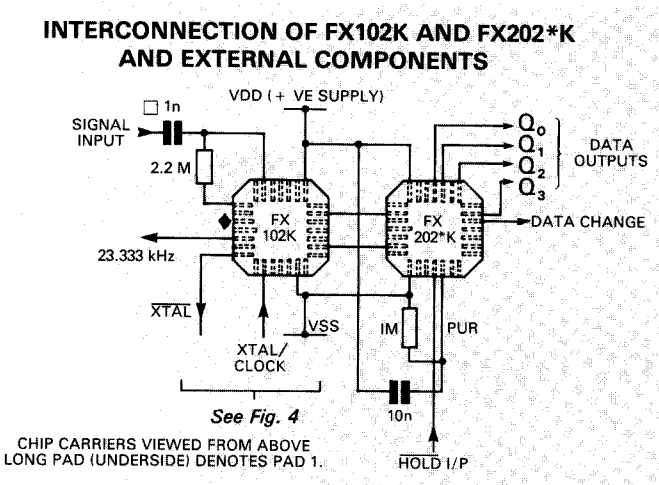



*Fig. 3 Chip Carrier*

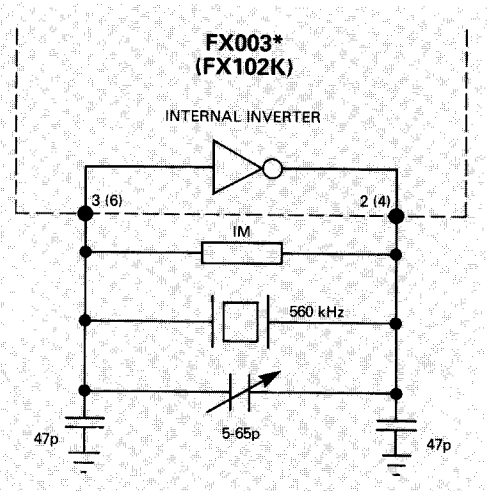



*Fig. 4 560 kHz Resonator Circuit*

## Character Tone Table

**Tone Frequencies ($f_O$) in Hz**

| 003QA (EIA) | 003QC (CCIR) | 003QE (EEA) | 003QZ (ZVEI) | 003QZS (ZVEI-S) | Output Code $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ | QTC Format Character |
|---|---|---|---|---|---|---|---|---|---|
| 600 | 1981 | 1981 | 2400 | 2400 | 0 | 0 | 0 | 0 | 0 |
| 741 | 1124 | 1124 | 1060 | 1060 | 0 | 0 | 0 | 1 | 1 |
| 882 | 1197 | 1197 | 1160 | 1160 | 0 | 0 | 1 | 0 | 2 |
| 1023 | 1275 | 1275 | 1270 | 1270 | 0 | 0 | 1 | 1 | 3 |
| 1164 | 1358 | 1358 | 1400 | 1400 | 0 | 1 | 0 | 0 | 4 |
| 1305 | 1446 | 1446 | 1530 | 1530 | 0 | 1 | 0 | 1 | 5 |
| 1446 | 1540 | 1540 | 1670 | 1670 | 0 | 1 | 1 | 0 | 6 |
| 1587 | 1640 | 1640 | 1830 | 1830 | 0 | 1 | 1 | 1 | 7 |
| 1728 | 1747 | 1747 | 2000 | 2000 | 1 | 0 | 0 | 0 | 8 |
| 1869 | 1860 | 1860 | 2200 | 2200 | 1 | 0 | 0 | 1 | 9 |
| 2151 | 2400 | 1055 | 2800 | 886 | 1 | 0 | 1 | 0 | A |
| 2433 | 930 | 930 | 810 | 810 | 1 | 0 | 1 | 1 | B |
| 2010 | 2247 | 2247 | 970 | 740 | 1 | 1 | 0 | 0 | C |
| 2292 | 991 | 991 | 886 | 680 | 1 | 1 | 0 | 1 | D |
| 459 | 2110 | 2110 | 2600 | 970 | 1 | 1 | 1 | 0 | E |
| NOTONE | NOTONE | NOTONE | NOTONE | NOTONE | 1 | 1 | 1 | 1 | F |

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | −0.3V to 7.0V |
| Input voltage at any pin (ref VSS = OV) | | −0.3V to (VDD + 0.3V) |
| Output sink/source current (total) | | 20mA |
| Operating temperature range: | FX003*<br>FX102K/FX202K* | −30°C to +85°C |
| Storage temperature: | FX003*<br>FX102K/FX202* | −55°C to 125°C |
| Maximum device dissipation | *QC, QZ, QE, QA, QZS | 100mW |

## Operating Limits

VDD = 5V, $T_A$ = 25°C, $\phi$ = 560kHz, $\Delta f \phi$ = 0.
All characteristics measured using the standard test circuit with the following test parameters, and is valid for all tones unless otherwise stated:—

| Characteristic | See Note | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Static Characteristics** | | | | | |
| Supply voltage (VSS = OV) | | 3.3 | 5.0 | 5.5 | V |
| Supply current | | | 500 | | μA |
| Logic '1' output I source = 0.1 mA | 1 | 4.5 | | | V |
| Logic '0' output I sink = 0.1 mA | 1 | | | 0.5 | V |
| Logic '1' input Level | 2 | 3.5 | | | V |
| Logic 'O' input level | 2 | | | 1.5 | V |
| **Dynamic Characteristics** | | | | | |
| Signal input range | 3 | 0.1 | | VDD | Vpk-pk |
| Decode Bandwidth (P⩾0.995) | 4 | | | | |
| QA | 4a | 20 | | | ±Hz |
| QC | 4b | 1 | | | ±% |
| QE | 4c | 1 | | | ±% |
| QZ/QZS | 4d | 2 | | | ±% |
| Not-decode bandwidth (P⩽0.03) | | | | | |
| QA | 5 | | | 60 | ±Hz |
| QC | 5 | | | 3 | ±% |
| QE | 5 | | | 3 | ±% |
| QZ/QZS | 5 | | | 4.5 | ±% |
| Noise response rate (hours per single character response with no input tone). F→ $\bar{F}$→ F | | | | | |
| QA | 6 | | 0.15 | | Hour |
| QC | 6 | | 40.0 | | Hour |
| QE | 6 | | 40.0 | | Hour |
| QZ/QZS | 6 | | 1.0 | | Hour |
| Decode response time: | | | | | |
| Notone to tone (F→ $\bar{F}$) | 7 | 20 | 25 | Tp | ms |
| Tone to notone, $T_f$ ($\bar{F}$→ F) | 7 | 33 | | 53 | ms |
| Min. intertone gap for 'F' | 8 | 15 | | 28 | ms |

**Notes**

1. *Relates to output pins 1, 8, 9-12.*
2. *Relates to input pins 5 and 6.*
3. *A.C. coupled, sine/squarewave.*
4. *With minimum tone period (Tp) specified for toneset. P = decode probability:*
   *(a), (c) SNR 3 dB*
   *(b), (d) SNR 0dB*
5. *All conditions of input SNR and amplitude with maximum Tp specified for toneset.*
6. *Gaussian input noise, bandwidth 6kHz, maximum input level corresponds to 1-digit code falsing rate. $\bar{F}$ = random single character.*
7. *Delay from change of input (tone applied/removed) to change at $Q_0 - Q_3$ outputs (see fig. 5).*
8. *Included in $T_2$. Minimum tone gap requirement for 'notone' recognition. Outputs = F after delay. (see fig. 5).*

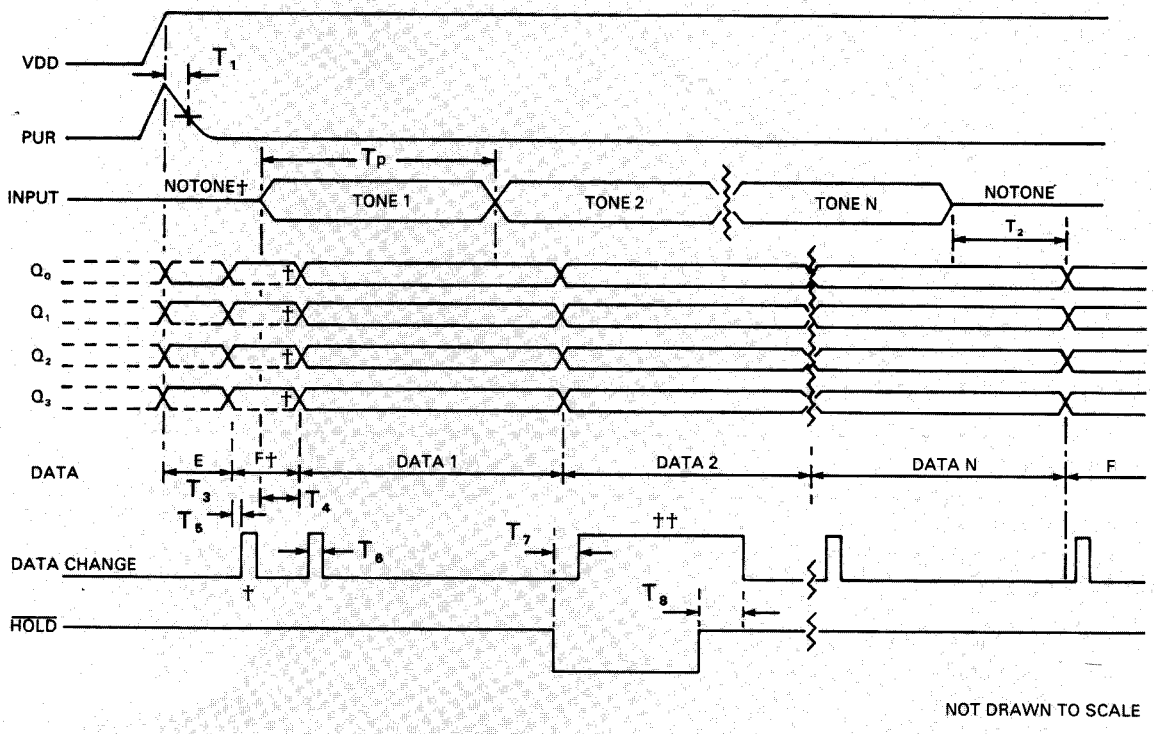



*Fig. 5 FX003* Timing Diagram (See References)* ** QC, QZ, QE, QA, QZS*

## Typical Performance

### References:

$T_1$ *Logic 1, > 2 ms*
$T_2$ *> 33 ms & < 50 ms*
$T_3$ *33 ms (DATA E)*
$T_4$ *20 ms minimum (Tp MAXIMUM)*
$T_5$ *0.5 ms — 1.0 ms (DATA CHANGE)*
$T_6$ *1.0 ms (DATA CHANGE PULSE DURATION)*
$T_7$ *> 50 μs*
$T_8$ *< 120 μs*

† *$Q_0$ — $Q_3$ will represent the input frequency present during and after PUR (shown as 'F' (Notone) in this example).*

†† *After application of $\overline{HOLD}$ the next Data Change pulse will stay high until $\overline{HOLD}$ is removed according to timing shown.*

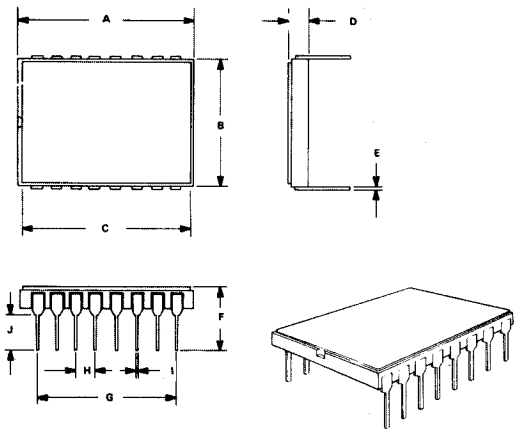
The ceramic dual-in-line package of the FX003 is shown in *Figure 6* and the chip carrier version shown in *Figure 7.* For the D.I.L. package, the pins number counter-clockwise (top view) from 1 with reference to a notch as a guidance. For the chip carrier package, pins number counter-clockwise (viewed from above) from the long pad (pad 1).

## Handling Precautions

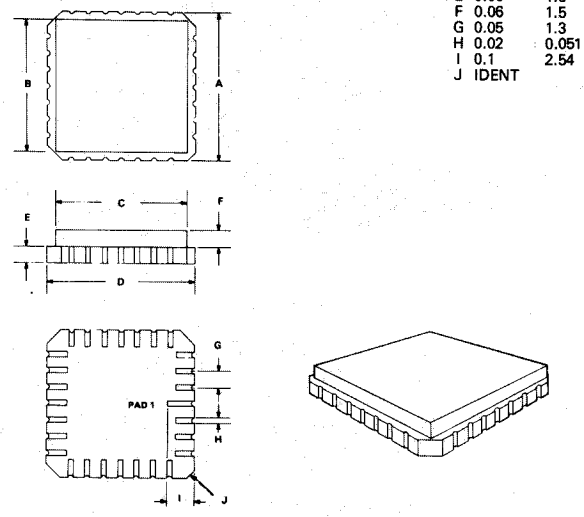
The FX003 is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which can cause damage.

Fig. 7 FX102K/202*K Chip Carrier Package

| | Inches | mm. |
|---|---|---|
| A | 0.80 | 20.32 |
| B | 0.59 | 15.00 |
| C | 0.77 | 19.56 |
| D | 0.11 | 2.79 |
| E | 0.01 | 0.25 |
| F | 0.30 | 7.62 |
| G | 0.70 | 17.78 |
| H | 0.10 | 2.54 |
| I | 0.018 | 0.46 |
| J | 0.155 | 3.94 |




| | Inches | mm. |
|---|---|---|
| A | 0.45 | 11.4 |
| B | 0.41 | 10.4 |
| C | 0.41 | 10.4 |
| D | 0.45 | 11.4 |
| E | 0.06 | 1.5 |
| F | 0.06 | 1.5 |
| G | 0.05 | 1.3 |
| H | 0.02 | 0.051 |
| I | 0.1 | 2.54 |
| J | IDENT | |




* *QC, QZ, QE, QA, QZS*

**FX003*** **16-pin Ceramic D.I.L.**
**FX102K** **28-pad Ceramic Chip Carrier**
**FX202*K** **28-pad Ceramic Chip Carrier**

*** VERSIONS**
**QC : CCIR**
**QZ : ZVEI**
**QE : EEA**
**QA : EIA**
**QZS : Suppressed ZVEI**

**Note:** *FX102K & FX202*K are available in pairs only.*

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