Technical Data

MC44BS373CA
Rev. 2.6, 6/2004

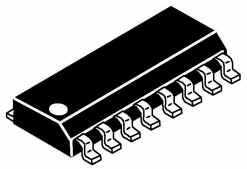
MC44BS373CA
Data Sheet

PLL-Tuned UHF and VHF Audio/Video High-Integration Modulator

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MC44BS373CA



SO16NB Package



QFN20 Package

Ordering Information

Device	Temp Range	Package
MC44BS373CAD,R2	–20 to +85°C	SO16NB
MC44BS373CAFC,R2	–20 to +85°C	QFN20 Lead Free
MC44BS373CAEF,R2	–20 to +85°C	SO16NB Lead Free
NOTE: For tape and reel, add R2 suffix.		

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The MC44BS373CA audio and video modulator is for use in VCRs, set-top boxes, and similar devices.

- Supports multiple standards
- TV output level 82 dBµV typical
- 5- and 3.3-V compatible I^2C bus

Figure 1 shows the pin connections for both package options.

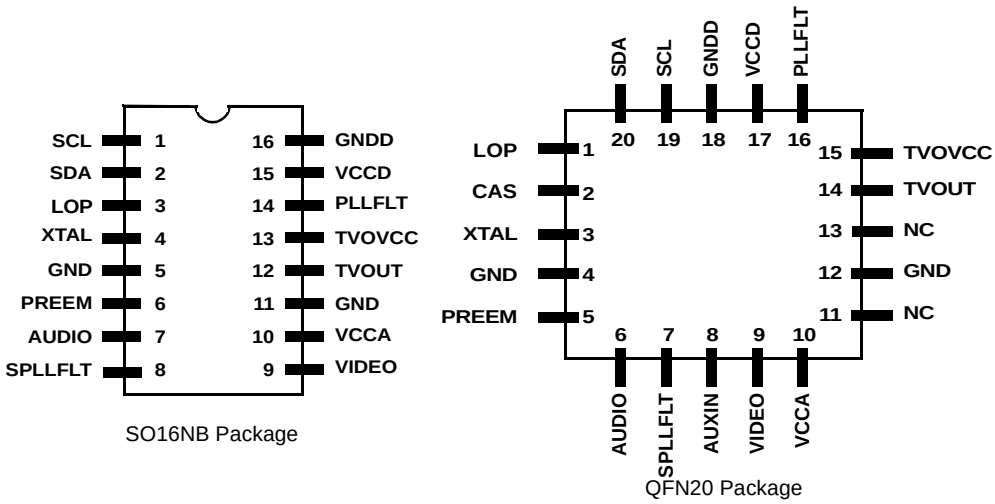


Figure 1. MC44BS373CA Pin Connections

1 Features

The MC44BS373CA is a multi-standard, PAL/SECAM/NTSC modulator.

The channel is set by an on-chip high-speed I^2C-compatible bus receiver. A phase-locked loop (PLL) tunes the modulator over the full UHF range.

The modulator incorporates a sound subcarrier oscillator and uses a second PLL to derive 4.5-, 5.5-, 6.0-, and 6.5-MHz subcarrier frequencies. These frequencies are selectable by bus.

The modulation standard can be chosen using a control bit that selects between positive and negative modulation.

The picture-to-sound ratio may be adjusted using the bus. In addition, an on-chip video test pattern generator can be switched on with a 1-kHz audio test signal.

The MC44BS373CA also has the following features:

- Integrated on-chip programmable UHF oscillator
- No external varicaps diodes/inductor or tuned components
- Extremely low external component count
- Channel 21–69 UHF operation
- VHF range possible by internal dividers (30–450 MHz)
- Boosted TVOUT level (82 dBµV typical)
- High-speed read and write I^2C bus compatible (800 kHz)
- I^2C address selectable by pin (four choices) using external resistor (available only in QFN20 package)
- I^2C bus 5- and 3.3-V compatible
- Fixed video modulation depth (93% typical in system L and 82% typical in the other standards)
- Peak white clip disabled by bus
- Programmable picture/sound carrier ratio (12 and 16 dB)
- Integrated on-chip programmable sound subcarrier oscillator (4.5, 5.5, 6.0 and 6.5 MHz)—no external varicaps
- Programmable sound reference frequency (31.25 and 62.5 kHz)
- Direct RF sound modulator input (FM and AM modulator bypassed) for NICAM or stereo sound applications (available only in QFN20 package)
- On-chip video test pattern generator with sound test signal (1 kHz)
- Low-power programmable modulator standby mode
- Transient output inhibit during PLL lock-up at power-on
- Logical output port controlled by bus
- ESD protection, minimum 4 KV

2 Comparing the MC44BS373CA to the MC44BC373/4C

Compared to the MC44BC373/4C devices, the MC44BS373CA has the following improvements:

- Higher output level (82 versus 74.5 dBµV)
- Higher video signal to noise (+3 dB)

- I^2C bus 3.3-V compatible
- Lower power consumption in normal and standby modes (–2 mA)
- Can be powered down without holding down I^2C lines
- TB1 bit no longer available (limited compatibility with MC44355 devices no longer available)
- New SREF bit to program sound reference frequency (31.25 and 62.5 kHz)
- Four different I^2C addresses selectable by single pin with external resistor (available only in QFN20 package)
- Direct sound RF modulator (FM and AM sound modulators bypassed) for NICAM or stereo sound applications (available only in QFN20 package)
- Switch between two integrated VCOs controlled directly by frequency divider (at 700 MHz)
- Lower RF second harmonic spurious but higher third harmonic spurious. In applications it is easier to filter UHF third harmonics spurious than second harmonics, as these frequencies are always out of the UHF band. Unfortunately, the second harmonic can fall back into the same UHF band (for instance channel 21 second harmonic). For this reason, it is almost impossible to have a good rejection of low UHF second harmonic with an external low-pass filter. This is why the design has been optimized for maximum second harmonic rejection in spite of an increase in the third harmonic level.

3 Pin Descriptions

This section describes the pins of the MC44BS373CA. First the 16-pin package will be considered, then the 20-pin package.

3.1 SO16 Package Pin Descriptions

The pins of the 16-pin package are listed in Table 1, along with a description of each.

Table 1. SO16 Package Pin Descriptions

Pin	Name	Description	Pin	Name	Description
1	SCL	I^2C clock	9	VIDEO	Video input
2	SDA	I^2C data	10	VCCA	Main analog supply voltage
3	LOP	Logical output port controlled by I^2C bus	11	GND	Analog ground
4	XTAL	Crystal	12	TVOUT	TV output signal
5	GND	Ground	13	TVOVCC	TV output stage supply voltage
6	PREEM	Pre-emphasis capacitor	14	PLLFLT	RF PLL loop filter
7	AUDIO	Audio input	15	VCCD	Digital supply voltage
8	SPLLFLT	Sound PLL loop filter	16	GNDD	Digital ground

3.2 QFN20 Package Pin Descriptions

The pins of the 20-pin package are listed in Table 2, along with a description of each.

Table 2. QFN20 Package Pin Descriptions

Pin	Name	Description
1	LOP	Logical output port controlled by I^2C bus
2	CAS	Chip address selection (external pull-down resistor or open)
3	XTAL	Crystal
4	GND	Ground
5	PREEM	Pre-emphasis capacitor
6	AUDIO	Audio input
7	SPLLFLT	Sound PLL loop filter
8	AUXIN	Sound auxiliary input (sound FM and AM modulators bypassed)
9	VIDEO	Video input
10	VCCA	Main analog supply voltage
11	NC	Not connected
12	GND	Analog ground
13	NC	Not connected
14	TVOUT	TV output signal
15	TVOVCC	TV output stage supply voltage
16	PLLFLT	RF PLL loop filter
17	VCCD	Digital supply voltage
18	GNDD	Digital ground
19	SCL	I^2C clock
20	SDA	I^2C data

4 MC44BS373CA Functional Overview

Figure 2 shows a simplified block diagram of the MC44BS373CA.

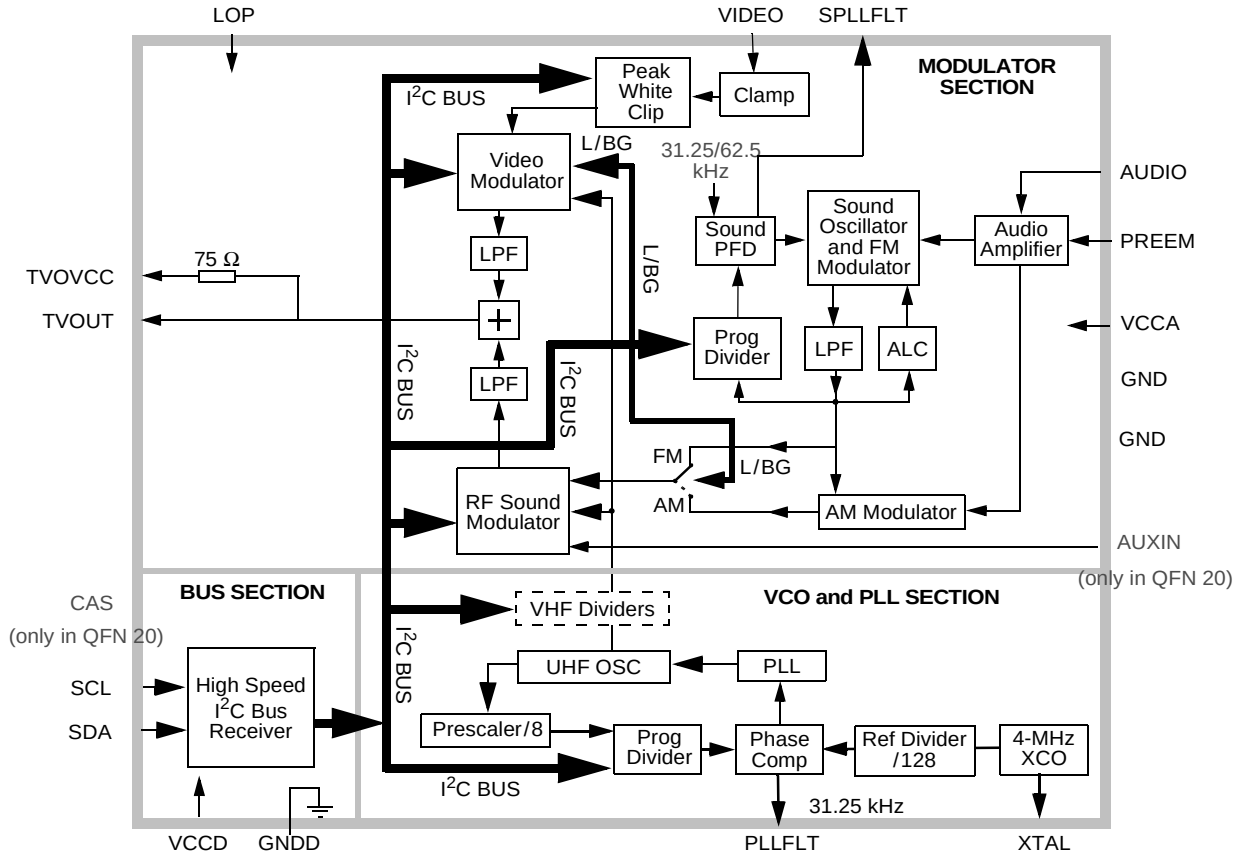


Figure 2. MC44BS373CA Simplified Block Diagram

The MC44BS373CA device has three main sections:

- A high-speed I^2C-compatible bus section
- A PLL section to synthesize the UHF/VHF output channel frequency (from an integrated UHF oscillator, divided for VHF output)
- A modulator section, which accepts audio and video inputs, then uses them to modulate the UHF/VHF carrier

An on-chip video test pattern generator with an audio test signal is included.

The MC44BS373CA operates as a multi-standard modulator and can handle the following systems using the same external circuit components: B/G, I, D/K, L, M/N.

High-frequency BiCMOS technology allows integration of the UHF tank circuit and certain filtering functions.

5 Maximum Ratings

Table 3 lists the maximum ratings supported for operating conditions of the MC44BS373CA.

NOTE

This device contains protection circuitry to guard against damage due to high-static voltage or electric fields. However, precautions must be taken to avoid applications of any voltages higher than maximum rated voltage to this high-impedance circuit. For proper operation, input and output voltages should be constrained to the ranges indicated in the recommended operating conditions.

Table 3. Maximum Ratings [1]

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	6	V
T_{amin}	Minimum operating ambient temperature	–20	°C
T_{amax}	Maximum operating ambient temperature	+85	°C
T_{stgmin}	Minimum storage temperature	–65	°C
T_{stgmax}	Maximum storage temperature	150	°C
T_j	Junction temperature	150	°C

[1] Maximum ratings are those values beyond which damage to the device may occur. For functional operation, values should be restricted to the recommended operating conditions.

Moisture sensitivity level ratings for the different packages are given in Table 4.

Table 4. Moisture Sensitivity Level Ratings (MSL)

Package	Rating	Dry Pack Required
MC44BS373CAD,R2	1	No
MC44BS373CAFC,R2 lead free packages	3	Yes
MC44BS373CAEF,R2 lead free packages	3	Yes

6 Thermal Ratings

Table 5 lists the junction-to-ambient thermal resistance for both packages.

Table 5. Thermal Resistance from Junction to Ambient

Symbol	Package	Value	Unit
R_{thja}	SO16NB	102	°C/W
R_{thja}	QFN20	120	°C/W

7 Electrostatic Discharge

Electrostatic discharge (ESD) tests are carried out on all pins using MIL STD 883C method 3015-7. Results are shown in Table 6.

Table 6. Electrostatic Discharge Tests

Symbol	Parameter	Minimum	Unit
ESD	MM (machine model)	400	V
ESD	HBM (human body model)	4000	V

8 Electrical Characteristics

Each of the operating conditions listed in Table 7 is characterized as one of the following types:

- A—100% tested
- B—100% correlation tested
- C—Characterized on samples
- D—Design parameter

See Section 14, “Characterization Measurement Conditions,” for each C-type parameter.

8.1 Operating Conditions

Unless otherwise stated, V_{CC} = 5.0 V, ambient temperature = 25°C, and video input is 1 Vp-p, with 10-step grey scale and RF output into 75-Ω load.

NOTE

Specifications are only valid for envelope demodulation.

Table 7. Operating Conditions

Parameter	Condition	Minimum	Typical	Maximum	Unit	Type	Notes
Operating supply voltage range	—	4.5	5.0	5.5	V	B	
Total supply current [1]	—	42	50	58	mA	A	1
Total standby mode supply current [2]	—	3	5	7	mA	A	2
Test pattern sync pulse width	—	3	4.7	6.5	µS	B	
Sound comparator charge pump current	During locking	7	10	12	µA	A	
	When locked	0.7	1	1.5			
RF comparator charge pump current	—	60	100	150	µA	A	
Crystal oscillator stability-negative resistance	—	1	—	—	KΩ	D	
Logic output port saturation voltage at I = 2 mA	—	—	160	300	mV	A	
Logic output port leakage current	—	—	—	1	µA		

[1] All sections active

[2] OSC = SO = ATT = 1, bus section active. See Section 15.3, “Standby Mode.”

9 I²C Bit Mapping

Table 8. I²C Write-Mode Bit Mapping

Write Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ACK
Chip address	1	1	0	0	1	See Table 11.		0	ACK
C1—High-order bits	1	0	SO	LOP	PS	X3	X2	SYSL	ACK
C0—Low-order bits	PWC	OSC	ATT	SFD1	SFD0	SREF	X5	X4	ACK
FM—High-order bits	0	TPEN	N11	N10	N9	N8	N7	N6	ACK
FL—Low-order bits	N5	N4	N3	N2	N1	N0	X1	X0	ACK

Table 9. I²C Read-Mode Bit Mapping

Read Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ACK
Chip address	1	1	0	0	1	See Table 12.		1	ACK
R—Status byte	—	—	—	—	—	Y2	Y1	OOR	—

Table 10. I²C Bit Mapping Bit Descriptions

Name	Description
SO	Sound oscillator on/off 0 Sound oscillator on (normal mode) 1 Sound oscillation disabled (oscillator and PLL section bias turned off)
LOP	Logic output port 0 LOP pin is low voltage. 1 LOP pin is high impedance.
PS	Picture-to-sound carrier ratio 0 Picture-to-sound carrier ratio is 12 dB. 1 Picture-to-sound carrier ratio is 16 dB.
X0–X5	Test mode bits Note: All bits are 0 for normal operation. For further information, see Table 17 and Table 18.
SYSL	System L enable—Selects AM sound and positive video modulation 0 System B/G enabled, system L disabled (FM sound and negative video modulation) 1 System L enabled, system B/G disabled (AM sound and positive video modulation)
PWC	Peak white clip enable/disable 0 Peak white clip on (system B/G) 1 Peak white clip off (system L)
OSC	UHF oscillator on/off 0 Normal operation 1 UHF oscillator disabled (oscillator and PLL sections bias turned off)
ATT	Modulator output attenuated-sound and video modulators on/off 0 Normal operation 1 Modulator output attenuation (sound and video modulators sections bias turned off)

Table 10. I²C Bit Mapping Bit Descriptions (continued)

Name	Description
SFD1 SFD0	Sound subcarrier frequency control bits SFD1 SFD0 Frequency 0 0 4.5 0 1 5.5 1 0 6.0 1 1 6.5
SREF	Sound PLL reference frequency 0 Sound reference frequency = 31.25 kHz 1 Sound reference frequency = 62.5 kHz
TPEN	Test pattern enable-picture and sound 0 Test pattern signal off (normal operation) 1 Test pattern signal on (picture and sound)
N0–N11	UHF frequency programming bits, in steps of 250 kHz See Section 15.7, “UHF PLL Section,” for more information.
Y2	RF oscillator operating range information 0 High VCO is active. 1 Low VCO is active.
Y1	RF oscillator operating range information 0 VCO out of range, frequency too low. Only valid if OOR=1 1 VCO out of range, frequency too high. Only valid if OOR=1
OOR	RF oscillator out-of-frequency range information 0 Normal operation, VCO in range 1 VCO out of range

Table 11 and Table 12 show how to select the I²C address.

NOTE

The I²C address is also selectable via the CAS pin. See Section 16, “High Speed I²C Compatible Bus,” for more information.

Table 11. I²C Address Selection, Write Mode

SFD1	SFD0	Address Selected	
		Binary	Hex
0	0	1100_1000	0xC8
1	0	1100_1010	0xCA
0	1	1100_1100	0xCC
1	1	1100_1110	0xCE

Table 12. I²C Address Selection, Read Mode

SFD1	SFD0	Address Selected	
		Binary	Hex
0	0	1100_1001	0xC9
1	0	1100_1011	0xCB
0	1	1100_1101	0xCD
1	1	1100_1111	0xCF

10 I²C Programming

The following tables list, by category, the bits used to program various parameters of the MC44BS373CA.

10.1 Sound Settings

Table 13 lists the sound settings used.

Table 13. Sound Settings

Bit	Value		Setting
Sound Subcarrier Frequency (MHz)			
SFD1 SFD0	**SFD1**	**SFD0**	
	0	0	4.5
	0	1	5.5
	1	0	6.0
	1	1	6.5
Picture-to-Sound Ratio (dB)			
PS	0		12
	1		16
Sound Oscillator			
SO	0		Sound oscillator on (normal mode)
	1		Sound oscillation disabled (oscillator and PLL section bias turned off)

Table 14 lists the video settings used.

Table 14. Video Settings

Bit	Value	Setting
System L/BG Selection		
SYSL	0	System B/G enabled, system L disabled (FM sound and negative video modulation)
	1	System L enabled, system B/G disabled (AM sound and positive video modulation)
Peak White Clip		
PWC	0	Peak white clip on (system B/G)
	1	Peak white clip off (system L)
Test Pattern Signal		
TPEN	0	Test pattern signal off (normal operation)
	1	Test pattern signal on (picture and sound)

Table 15 lists the UHF settings used.

Table 15. UHF Settings

Bit	Value	Setting
UHF Oscillator		
OSC	0	Normal operation
	1	UHF oscillator disabled (oscillator and PLL sections bias turned off)
Modulator Output Attenuation		
ATT	0	Normal operation
	1	Modulator output attenuation (sound and video modulators sections bias turned off)

Table 16 lists the other settings used.

Table 16. Other Settings

Bit	Value	Setting
Sound PLL		
SREF	0	Sound reference frequency = 31.25 kHz.
	1	Sound reference frequency = 62.5 kHz.
Logic Output Port		
LOP	0	LOP pin is low voltage.
	1	LOP pin is high impedance.
Standby Mode		
OSC SO ATT	1, 1, 1	Puts the MC44BS373CA into standby mode. See Section 15.3, “Standby Mode,” for more information.

Table 17 lists settings of fields X2, X1, and X0, used to set the device into test mode 1 and to control the VHF range.

NOTE

Test modes 1 and 2 are intended for manufacturing test purposes only and cannot be used for normal applications, except for VHF range (states 1.b to 1.e).

Table 17. Write Mode—Test Mode 1 and VHF Range

X2	X1	X0	State	Description
0	0	0	1.a	Normal operation
0	0	1	1.b	RF frequency divided for low-frequency testing or VHF range: RF/2
0	1	0	1.c	RF/4
0	1	1	1.d	RF/8
1	0	0	1.e	RF/16

Table 17. Write Mode—Test Mode 1 and VHF Range (continued)

X2	X1	X0	State	Description
1	0	1	1.f	DC drive applied to modulators—Non-inverted video at TVOUT
1	1	0	1.g	DC drive applied to modulators—Inverted video at TVOUT
1	1	1	1.h	Transient output inhibit disabled (that is, speed-up mode) During this speed-up test mode, ATT = 0 forces sound current source to 1 μA, while ATT = 1 forces it to 10 μA.

Table 18 lists settings of fields X5, X4, and X3, used to set the device into test mode 2.

Table 18. Write Mode—Test Mode 2

X5	X4	X3	State	Description
0	0	0	2.a	Normal operation
0	0	1	2.b	Test pattern generator DC verification (test pattern DC test mode available)
0	1	0	2.c	Program divider test (UHF program divider on PLLFILT pin and sound program divider on SPLLFIL pin)
0	1	1	2.d	Reference divider test (UHF reference divider on PLLFILT pin)
1	0	0	2.e	UHF phase comparison, upper source on PLLFILT pin Sound phase comparison 10-μA upper source on SPLLFIL (only valid during transient output inhibit)
1	0	1	2.f	UHF phase comparison, lower source on PLLFILT pin Sound phase comparison 10-μA lower source on SPLLFIL (only valid during transient output inhibit)
1	1	0	2.g	Sound phase comparison 1-μA upper source on SPLLFIL (not valid during transient output inhibit)
1	1	1	2.h	Sound phase comparison 1-μA lower source on SPLLFIL (not valid during transient output inhibit)

Table 19 lists settings of fields Y2, Y1, and OOR, used to set the device into READ mode and to determine RF oscillator out-of-frequency range information.

Table 19. Read Mode

Bit	Value	Setting
OOR	0	Normal operation, VCO in range
	1	VCO out of range
Y1	0	VCO out of range, frequency too low. Only valid if OOR=1
	1	VCO out of range, frequency too high. Only valid if OOR=1
Y2	0	High VCO is active.
	1	Low VCO is active.

11 Modulator High-Frequency Characteristics

Each of the characteristics listed in Table 20 is classified as one of the following types:

- A—100% tested
- B—100% correlation tested
- C—Characterized on samples
- D—Design parameter

See Section 14, “Characterization Measurement Conditions,” for each C-type parameter.

Unless otherwise stated, V_{CC} = 5.0 V, ambient temperature = 25°C, and video input is 1 Vp-p, with 10-step grey scale and RF output into 75-Ω load.

NOTE

Specifications only valid for envelope demodulation.

Table 20. High-Frequency Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit	Type	Notes
TVOUT output level	Output signal from modulator section	79	82	85	dBµV	B	1, 2
UHF oscillator frequency	—	460	—	880	MHz	A	
VHF range	From UHF oscillator internally divided	45	—	460	MHz	B	
TVOUT output attenuation	During transient output inhibit, or when ATT bit is set to 1	65	75	—	dBc	B	1, 2
Sound subcarrier harmonics (Fp + n × Fs)	Reference picture carrier	50	63	—	dBc	C	1
Second harmonic of chroma subcarrier	Using red EBU bar	45	70	—	dBc	C	1
Chroma/sound intermodulation: Fp + (Fsnd – Fchr)	Using red EBU bar	65	82	—	dBc	C	1
Fo (picture carrier) harmonics	2nd harmonic: CH21	—	38	50	dBµV	C	1,3
	3rd harmonic: CH21	—	58	70			
	Other channels	—					2
Out-of-band (picture carrier) spurious	1/2 × Fo – 1/4 × Fo – 3/2 × Fo – 3/4 × Fo From 40 MHz to 1 GHz.	—	—	10	dBµV	C	1
In-band spurious (Fo at 5 MHz)	No video sound modulation.	65	75	—	dBc	C	1

Notes:

1. See Section 14, “Characterization Measurement Conditions.”
2. See Figure 3.
3. Picture carrier harmonics are highly dependent on PCB layout and decoupling capacitors.

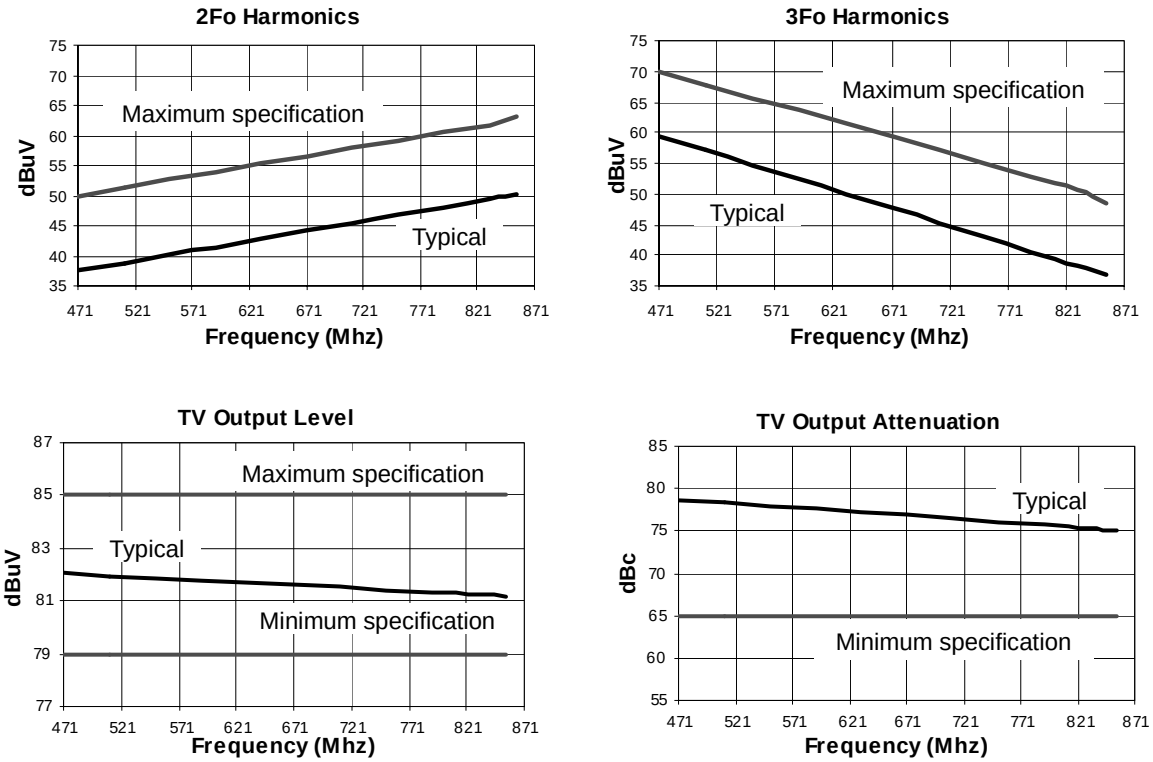


Figure 3. Typical High-Frequency Performance

12 Video Characteristics

Each of the characteristics listed in Table 21 is classified as one of the following types:

- A—100% tested
- B—100% correlation tested
- C—Characterized on samples
- D—Design parameter

See Section 14, “Characterization Measurement Conditions,” for each C-type parameter.

Unless otherwise stated, V_{CC} = 5.0 V, ambient temperature = 25°C, and video input is 1 Vp-p, with 10-step grey scale and RF output into 75-Ω load.

NOTE

Specifications are only valid for envelope demodulation.

Table 21. Video Performance Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit	Type	Notes
Video bandwidth	Reference 0 dB at 100 kHz, measured at 5 MHz.	–1.5	–0.8	—	dB	C	1
Video input level	75-Ω load	—	—	1.5	V_{CVBS}	D	
Video input current		—	0.2	1	µA	A	

Table 21. Video Performance Characteristics (continued)

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit	Type	Notes
Video input impedance		500	—	—	KΩ	A	
Peak white clip	Video modulation depth for video = 1.4 V_{CVBS}	90.5	94	97.5	%	B	
Video S/N	No sound modulation,100% white video						
	Using CCIR Rec.567 weighting filter	53	56	—	dB	C	1, 2
	Unweighted	48	53	—		C	1
Differential phase	CCIR test line 330, worst case from first 4 steps out of 5	–5	—	5	deg	C	1
Differential gain	CCIR test line 330, worst case from first 4 steps out of 5	–5	—	5	%	C	1
Luma/Sync ratio	Input ratio 7.0:3.0	6.8/3.2	7.0/3.0	7.2/2.8	—	B	
PAL video modulation depth (SYSL = 0)		76	82	88	%	B	1, 2
SECAM video modulation depth (SYSL = 1)		87	93	99	%	B	1, 2

Notes:

1. See Section 14, “Characterization Measurement Conditions.”
2. See Figure 4.

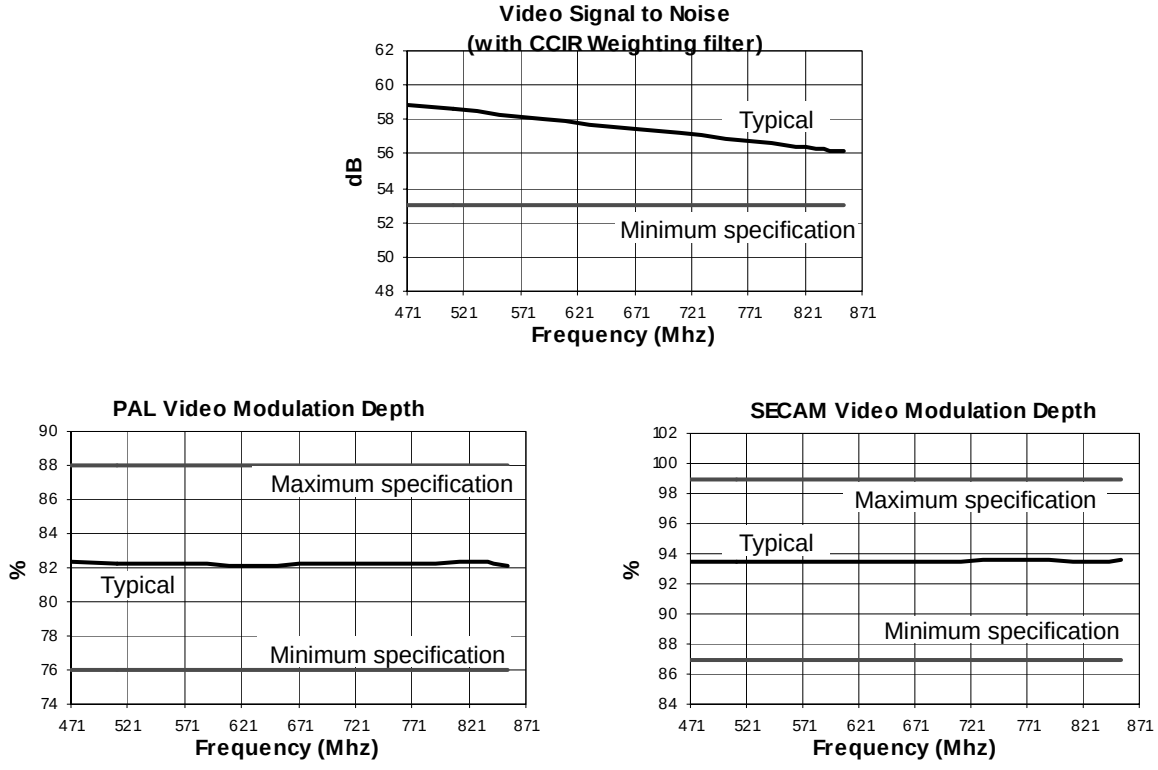


Figure 4. Typical Video Performance

13 Audio Characteristics

Each of the characteristics listed in Table 22 is classified as one of the following types:

- A—100% tested
- B—100% correlation tested
- C—Characterized on samples
- D—Design parameter

See Section 14, “Characterization Measurement Conditions,” for each C-type parameter.

Unless otherwise stated, V_{CC} = 5.0 V, ambient temperature = 25°C, and video input is 1 Vp-p, with 10-step grey scale and RF output into 75-Ω load.

NOTE

Specifications are only valid for envelope demodulation.

Table 22. Audio Performance Characteristics [1]

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit	Type
Picture-to-sound ratio	PS bit set to 1	13	16	19	dB	B
	PS bit set to 0	9	12	15		
Audio modulation depth	Using specific pre-emphasis circuit, audio input level = 205 mVrms, audio frequency = 1 kHz					
	AM modulation: SECAM Fs=6.5MHz	76	80	84	%	B
	FM modulation: Fs=5.5, 6, or 6.5 MHz 100% modulation = ±50 kHz FM deviation	76	80	84	%	B
	FM modulation: NTSC Fs=4.5MHz 100% modulation = ±25 kHz FM deviation	76	80	84	%	B
Audio input resistance		45	53	61	KΩ	A
Audio frequency response	Reference 0dB at 1kHz using specified pre-emphasis circuit, measured from 50 Hz to 15 kHz (depends on loop filter components)	–2.0	—	+2.0	dB	C
Audio distortion FM (THD only)	At 1 kHz, 100% modulation (±50 kHz) No video	—	0.2	0.8	%	C
Audio distortion AM (THD only)	At 1 kHz, 100% modulation No video	—	1.5	2.5	%	D
Audio S/N with sync buzz FM	Ref 1 kHz, 50% modulation (±25 kHz) EBU color bars video signal, using CCIR 468-2 weighting filter	50	54	—	dB	C
Audio S/N with sync buzz AM	Reference 1kHz, 85% modulation Video input EBU color bar 75% Audio BW 40Hz–15kHz, using CCIR 468-2 weighting filter	45	50	—	dB	D

[1] See Section 14, “Characterization Measurement Conditions.”

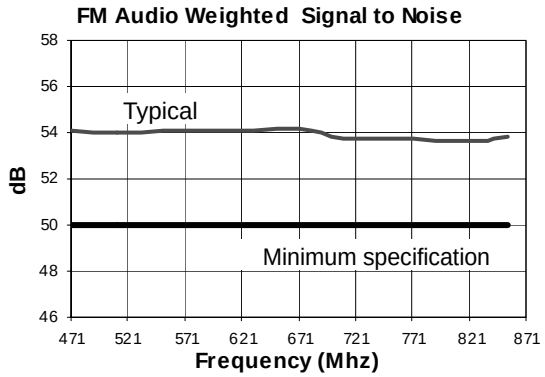


Figure 5. Typical Audio Performance

14 Characterization Measurement Conditions

Table 23 shows the MC44BS373CA default configuration unless otherwise specified.

Table 23. Device Default Configuration

Device Feature	Default Setting
Peak white clip	Enabled
UHF oscillator	On
Sound and video modulators	On
Sound subcarrier frequency	5.5 MHz
Sound oscillator	On
Sound PLL reference frequency	31.25 kHz
Logic output port	Low
Picture-to-sound carrier ratio	12 dB
System L	Disabled
Test pattern	Disabled
All test mode bits	Zero
Frequency	From channel 21 to 69

RF inputs/output into 75-Ω load using a 75- to 50-Ω transformation. Video input 1 Vp-p. Audio pre-emphasis circuit enabled.

Table 24. Measurement Conditions

Device and Signal Set-Up	Measurement Set-Up
TVOUT Output Level	
Video: 10-step grey scale No audio	Measured picture carrier in dBµV with the HP8596E spectrum analyzer using a 75- to 50-Ω transformation, all cable losses and transformation pads having been calibrated. Measurement used as a reference for other tests: TVout_Ref

Table 24. Measurement Conditions (continued)

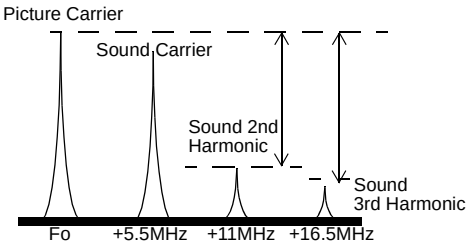
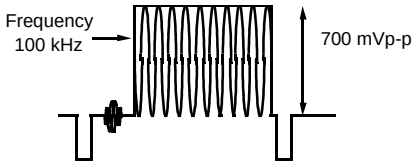
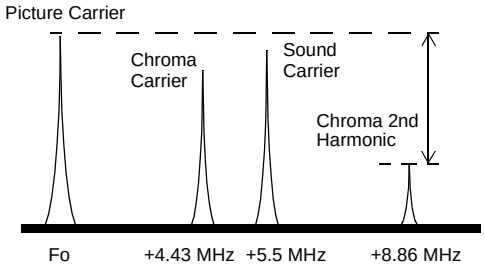
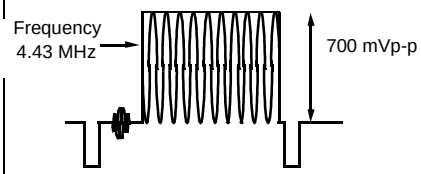
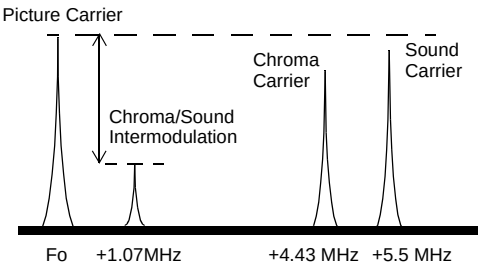
Device and Signal Set-Up	Measurement Set-Up
TVOUT Output Attenuation	
ATT bit = 1 No video signal No audio signal	Measure in dBc picture carrier at ATT = 1 with reference to picture carrier at ATT = 0
Sound Subcarrier Harmonics	
Video: 10-step grey scale No audio signal	Measure in dBc second and third sound harmonics levels in reference to picture carrier (TVout_Ref). 
Second Harmonics of Chroma Subcarrier	
No audio Video: a 700-mVp-p, 100-kHz sinusoidal signal is inserted on the black level of active video area. 	Measure in dBc, in reference to picture carrier (TVout_Ref), second harmonic of chroma at channel frequency plus two times chroma frequency, resulting in the following spectrum. 
Chroma/Sound Intermodulation	
No audio signal Video: a 700-mVp-p, 100-kHz sinusoidal signal is inserted on the black level of active video area.This is generated using a Rohde & Schwarz video generator SAF and inserting the required frequency from an RF signal generator. 	Measure in dBc, in reference to picture carrier (TVout_Ref), intermodulation product at channel frequency plus the sound carrier frequency (+5.5 MHz) minus the chroma frequency (–4.43 MHz), resulting in the following spectrum (Intermodulation product is at the channel frequency +1.07 MHz): 

Table 24. Measurement Conditions (continued)

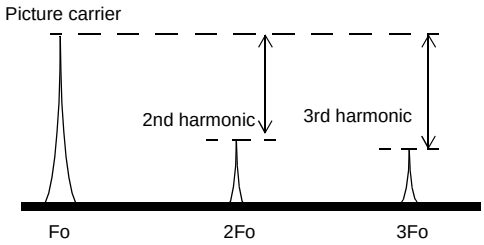
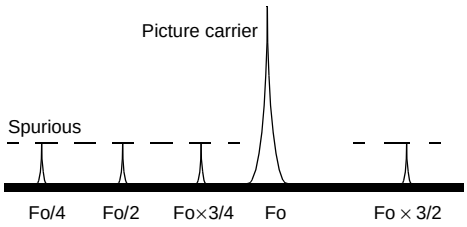
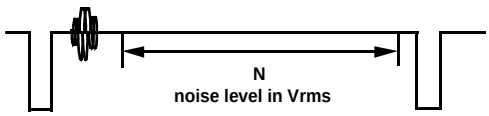
Device and Signal Set-Up	Measurement Set-Up
Picture Carrier Harmonics	
No video signal No audio signal	Measure in dBc, in reference to picture carrier (TVout_Ref), second and third harmonic of channel frequency, resulting in the following spectrum 
Out-of-Band Spurious	
No video signal No audio signal	Measure in dBµV spurious levels at 0.25, 0.5, 0.75 and 1.5 times channel frequency, resulting in the following spectrum (measure from 40 MHz to 1 GHz): 
In-Band Spurious	
No video signal No audio signal	Measure in dBc, in reference to picture carrier (TVout_Ref), spurious levels falling into video bandwidth starting from ±100 kHz from the picture carrier up to ±5MHz.
Video Bandwidth	
No audio Video: 600-mVp-p sinusoidal signal inserted on the black level of active video area	The video signal is demodulated on the spectrum analyzer, and the peak level of the 100-kHz signal is measured as a reference. The frequency is then swept from 100 kHz to 5 MHz, and then the difference in dB from the 100-kHz reference level is measured.
Weighted Video Signal to Noise	
Video: 100% white video signal, 1 Vp-p. No audio signal This is measured using a Rohde & Schwarz AMFS UHF demodulator in B/G (using a CCIR Rec. 567 weighting network), 100-kHz to 5-MHz band with sound trap and envelope detection, and a Rohde & Schwarz UAF video analyzer.	The video analyzer measures the ratio between the amplitude of the active area of the video signal (700 mV) and the noise level in Vrms on a video black level which is shown below. Video S/N is calculated as 20 x log(700/N) in dB. 

Table 24. Measurement Conditions (continued)

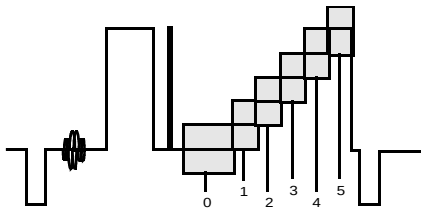
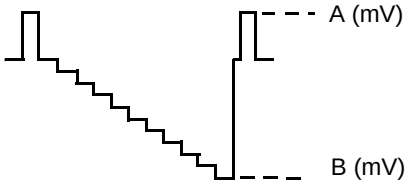
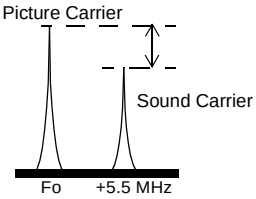
Device and Signal Set-Up	Measurement Set-Up
Unweighted Video Signal to Noise	
Same as above with CCIR filter disabled	Same as above
Video Differential Phase	
Video: 5-step grey scale, 1 Vp-p No audio signal This is measured using a Rohde & Schwarz AMFS UHF demodulator in B/G (using a CCIR Rec. 567 weighting network), 100-kHz to 5-MHz band with sound trap and envelope detection, and a Rohde & Schwarz UAF video analyzer.	On line CCIR 330, the video analyzer DP measure consists of calculating the difference of the chroma phase at the black level and the different chroma subcarrier phase angles at each step of the grey scale. The largest positive or negative difference indicates the distortion. $\text{Diff Phase} = \frac{\text{Largest positive or negative difference}}{\text{Phase at position 0}} \times 100\%$ The video analyzer method takes the worst step from the first 4 steps.
Video Differential Gain	
Video: 5-step grey scale, 1 Vp-p No audio signal This is measured using a Rohde & Schwarz AMFS UHF demodulator in B/G (using a CCIR Rec. 567 weighting network), 100-kHz to 5-MHz band with sound trap and envelope detection, and a Rohde & Schwarz UAF video analyzer.	On line CCIR 330 shown below, the video analyzer DG measure consists of calculating the difference of the chroma amplitude at the black level and the different amplitudes at each step of the grey scale. The largest positive or negative difference indicates the distortion.  5-Step Grey Scale with Chroma Subcarrier Superimposed (Not to Scale), Line CCIR 330 $\text{Diff Gain} = \frac{\text{Largest positive or negative difference}}{\text{Amplitude at position zero}} \times 100\%$ The video analyzer method takes the worst step from the first 4 steps.
Video Modulation Depth	
No audio signal Video: 10-step grey scale	This is measured using an HP8596E spectrum analyzer with a TV trigger option, allowing demodulation and triggering on any specified TV line. The analyzer is centred on the maximum peak of the video signal and reduced to 0 Hz span in linear mode to demodulate the video carrier  TV Line Demodulated by Spectrum Analyzer—BG Standard The modulation depth is calculated as (A – B) / A x 100 in percent. Same measurement method for L standard, with inverted video.

Table 24. Measurement Conditions (continued)

Device and Signal Set-Up	Measurement Set-Up
Picture-to-Sound Ratio	
No video signal No audio signal PS bit set to 0 and 1	Measure in dBc sound carrier in reference to picture carrier (TVout_Ref) for PS bit = 0 (PS = 12 dB typical) and for PS bit = 1 (PS = 16 dB), 
Audio Modulation Depth—FM Modulation	
Video black level Audio signal: 1 kHz, 205 mVrms. This is measured using a Rohde & Schwarz AMFS demodulator in B/G and an HP8903A audio analyzer at 1 kHz.	The audio signal, 205 mV at 1 kHz, is supplied by the audio analyzer, and the FM demodulated signal deviation is indicated on the demodulator in kHz peak. This value is then converted into percentage of FM deviation, based on specified standards.
Audio Frequency Response	
Video black level Audio signal: 50 Hz to 15 kHz, 100 mVrms This is measured using a Rohde & Schwarz AMFS demodulator in B/G and an HP8903A audio analyzer.	The audio signal, 1 kHz 100 mVrms, is supplied by the audio analyzer, and demodulated by the demodulator. The audio analyzer measures the AC amplitude of this demodulated audio signal. This value is taken as a reference (0 dB). The audio signal is then swept from 50 Hz to 15 kHz and demodulated. AC amplitude is measured in dB relative to the 1-kHz reference. Audio pre-emphasis and de-emphasis circuits are engaged and all audio analyzer filters are switched off.
Audio Distortion FM	
Audio: 1 kHz, adjustable level Video black level This is measured using a Rohde & Schwarz AMFS UHF demodulator in B/G and an HP8903A audio analyzer at 1 kHz. The output level of the audio analyzer is varied to obtain a deviation of 50 kHz indicated on the demodulator.	The input arms detector of the audio analyzer converts the AC level of the combined signal + noise + distortion to DC. It then removes the fundamental signal (1 kHz) after having measured the frequency. The output rms detector converts the residual noise + distortion to DC. The DC voltmeter measures both DC signals and calculates the ratio of the two signals as a percentage. $ADist = (Distortion + Noise)/(Distortion + Noise + Signal)$
Audio Signal to Noise	
Audio: 1 kHz, adjustable level Video: EBU color bars This is measured using a Rohde & Schwarz AMFS demodulator in B/G and an HP8903A audio analyzer at 1 kHz. The output level of the audio analyzer is varied to obtain a modulation deviation of 25 kHz indicated on the AMFS demodulator.	The audio analyzer alternately turns on and off its internal audio source to make a measure of the audio signal plus noise and then another measure of only the noise. The measurement is made using the internal CCIR 468-2 filter of the audio analyzer together with the internal 30±2-kHz (60 dB/decade) low-pass filters. The AMFS demodulator uses a quasi-parallel demodulation as is the case in a normal TV set. In this mode the Nyquist filter is bypassed and the video carrier is used without added delay to effectuate intercarrier conversion. In this mode the phase noise information fully cancels out and the true S/N can be measured. $ASN(dB) = 20 \times \log(Signal + Noise)/(Noise)$

15 MC44BS373CA Modes of Operation

15.1 Power-On Settings

At power on, the MC44BS373CA is configured as shown in Table 25 below.

Table 25. Power-On Settings

WRITE MODE	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ACK
C1-High order bits	1	0	0	0	0	0	0	0	ACK
C0-Low order bits	0	0	0	0	1	0	0	0	ACK
FM-High order bits	0	0	N11	N10	N9	N8	N7	N6	ACK
FL-Low order bits	N5	N4	N3	N2	N1	N0	0	0	ACK

Note:
N0 to N11 are set to have UHF oscillator on channel E36 (591.25 MHz). (See Section 15.7, “UHF PLL Section,” for more information.) Peak white clip is on. Sound frequency is 5.5 MHz. Sound reference frequency is 31.25 kHz. Logic output port is low voltage. Picture-to-sound ratio is 12 dB.

15.2 Power Supply

The three device V_{CC} pins (pins 10, 13 and 15 for SO16 package, pins 10, 15 and 17 for QFN20 package) must be applied at the same time to ensure all internal blocks are correctly biased. Do not bias any other pin before V_{CC} is applied to the MC44BS373CA.

When all V_{CC}s are switched to 0 V, the SDA and SCL pins are high impedance.

15.3 Standby Mode

During standby mode, the modulator is switched to low power consumption. That is, the sound oscillator, UHF oscillator, and the video and sound modulator sections’ bias are internally turned off. The I^2C bus section remains active.

The MC44BS373CA can be set to standby mode with a combination of 3 bits: OSC = 1, SO = 1, and ATT = 1.

15.4 System L or B/G Selection

The SYSL pin can be used to switch the device between system L and system B/G, as summarized in Table 26.

Table 26. System L or B/G Selection

Function	B/G (SYSL = 0)	L (SYSL = 1)
Video modulation polarity	Negative	Positive
Video modulation depth (% typical) [1]	82	93
Sound modulation	FM	AM

[1] See Section 12, “Video Characteristics.”

15.5 Transient Output Inhibit

To minimize the risk of interference to other channels while the UHF PLL is acquiring a lock on the desired frequency, the sound and video modulators are turned off during a timeout period for the following cases:

- Power-on from zero (that is, all V_{CC} switched from 0 to 5 V)
- UHF oscillator power-on from off state (that is, OSC bit switched from 1 to 0)

There is a timeout of 263 ms until the output is enabled. This lets the UHF PLL settle to its programmed frequency. During the 263-ms timeout, the sound PLL current source is set to 10 µA typical to speed up the locking time. After the timeout, the current source is switched to 1 µA. Use care when selecting loop filter components to ensure the loop transient does not exceed this delay.

For test purposes, it is possible to disable the 263-ms delay using test mode 1, state 1.h. (This is called speed-up mode.) Table 17 provides settings pertaining to test mode 1.

15.6 UHF Oscillator—VHF range

The UHF oscillator is fully integrated and does not require any external components.

For low-frequency testing or VHF range operation (test mode 1, states 1.b to 1.e) the UHF oscillator can be internally divided by 2, 4, 8, or 16.

15.7 UHF PLL Section

The reference divider is a fixed divide-by-128, resulting in a reference frequency of 31.25 kHz with a 4.0-MHz crystal.

The prescaler is a fixed divide-by-8 and is permanently engaged.

The programmable divider division ratio is controlled by the state of control bits N0 to N11.
The divider ratio N for a desired frequency F (in MHz) is given by:

$$N = \frac{F}{8} \times \frac{128}{4}$$

with:

$$N = 2048 \times N11 + 1024 \times N10 + \ldots\ldots + 4 \times N2 + 4 \times N1 + N0$$

NOTE

Programming a division ratio of N = 0 is not allowed.

15.8 Logic Output Port (LOP)

The LOP pin controls any logic function. The primary applications for LOP are to control an external attenuator or an external switch between the antenna input and TV output. A typical attenuator application with PIN diode is shown in Figure 6. The LOP pin switches the PIN attenuator depending on the signal strength of the antenna input. This reduces the risk of intermodulation in certain areas. The LOP can also be used as an off position bypass switch or for other logic functions in the application.

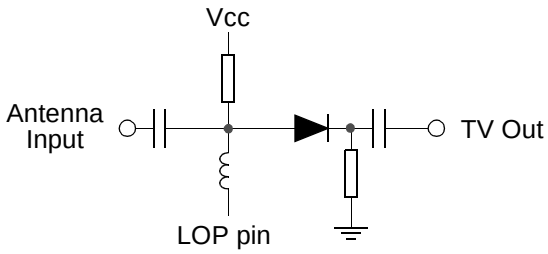


Figure 6. Typical Attenuator Application with Pin Diode

15.9 Video Section—Peak White Clip

The MC44BS373CA requires the following for proper video functionality:

- A composite video input with negative going sync pulses
- A nominal level of 1 Vp-p

This signal is AC-coupled to the video input where the sync tip level is clamped.

The video signal is then passed to a peak white clip (PWC) circuit. The PWC circuit function soft-clips the top of the video waveform, if the sync tip amplitude to peak white clip goes too high. This avoids carrier over-modulation by the video. Clipping can be disabled by software.

15.10 Test Pattern Generator

The I^2C generates a simple test pattern, which can be switched under bus control to permit a TV receiver to easily tune to the modulator output. The pattern consists of two white vertical bars on a black background and a 976-Hz audio test signal.

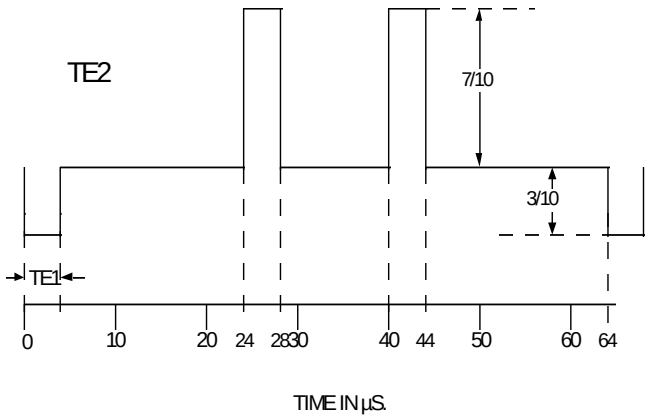


Figure 7. Test Pattern Generator

15.11 Sound Section

The oscillator is fully integrated and does not require any external components. An internal low-pass filter and matched structure provide very low harmonics levels.

The sound modulator system consists of an FM modulator incorporating the sound subcarrier oscillator. The audio input signal is AC-coupled into the amplifier, which then drives the modulator. For mono applications, the audio pre-emphasis circuit is a high-pass filter with an external capacitor and an internal resistor (106 KΩ typical).

The recommended capacitor value for BG standard (with a time constant of 50 µS) is 470 pF.

The recommended capacitor value for M/N standard (with a time constant of 75 µS) is 750 pF.

The sound reference divider is a programmable divide-by-128 or divide-by-64, resulting in a reference frequency of 31.25 kHz or 62.5 kHz with a 4.0-MHz crystal.

This reference frequency can be selected by bus (bit SREF), depending on the application. For instance, when the audio bandwidth is required to be extended (for stereo application), it is possible to select the higher value (62.5 kHz) to avoid any interference between the reference and the audio signals.

For stereo applications, the audio signal is already encoded in the baseband stereo encoder. It is not necessary to use a pre-emphasis, and in this case the pre-emphasis capacitor must be removed.

Sometimes for the same application it is useful to increase the FM deviation. To increase FM deviation, replace the original pre-emphasis capacitor with a fixed 100-nF capacitor. Adding this value boosts the deviation and does not create a pre-emphasis.

Without pre-emphasis, the audio bandwidth extends to 60 kHz.

To increase the audio bandwidth at low frequencies it is recommended to change the sound PLL loop filter. It is also recommended to increase the values of the loop filter capacitors. The recommended values are 1 µF and 100 nF.

It is possible to create a peak for the low frequencies (from 30 to 80 Hz) by adjusting the resistor of the sound loop filter. A flat response is given with a value of 5.6 KΩ but this value can be set to 4.7 KΩ. This gives a peak of about 1 dB at 40 Hz and extends the low-frequency cut-off to 28 Hz.

The following figure plots the resulting bandwidth for low frequencies and for the whole bandwidth (up to 60 kHz).

The first chart represents the audio bandwidth for low frequencies (20 to 150 Hz) for two sets of sound loop filters. The first set with 1 µF + 100 nF + 5.6 KΩ gives a flat response. The second set with 1 µF + 100 nF + 4.7 KΩ gives a peak of about 1 dB at 60 Hz. It is possible to adjust this peak by changing the resistor value.

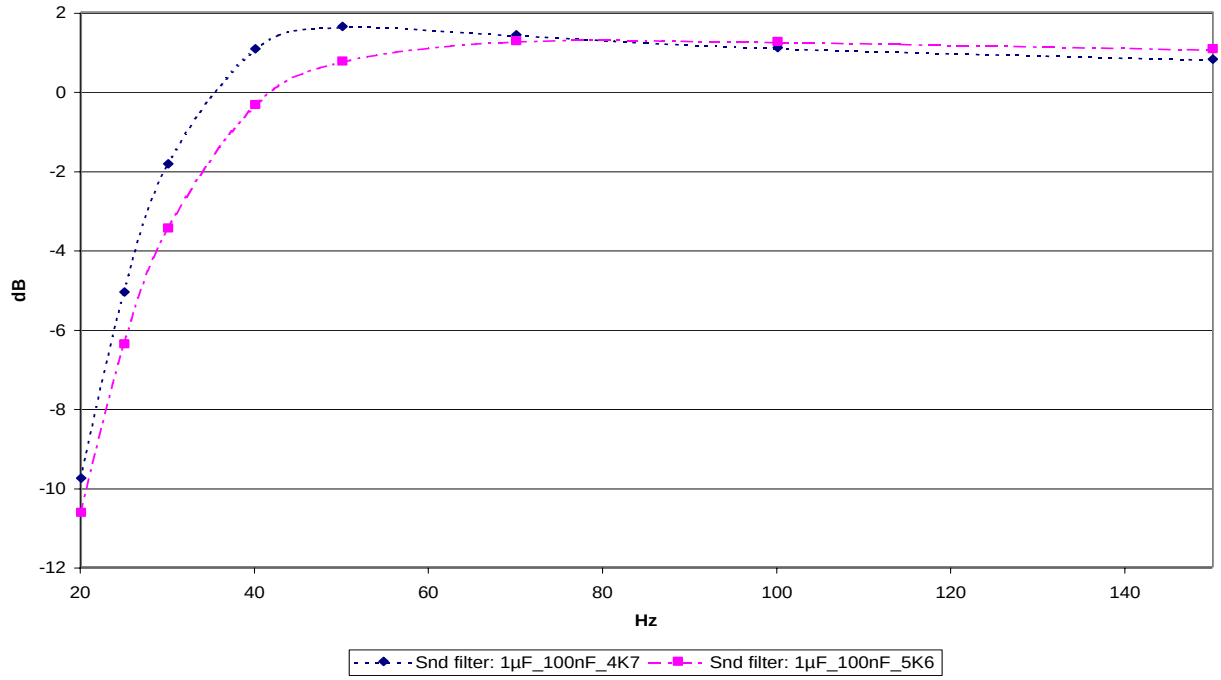


Figure 8. Audio Bandwidth Measurements (20 Hz to 150 Hz) Versus Loop Filter Components

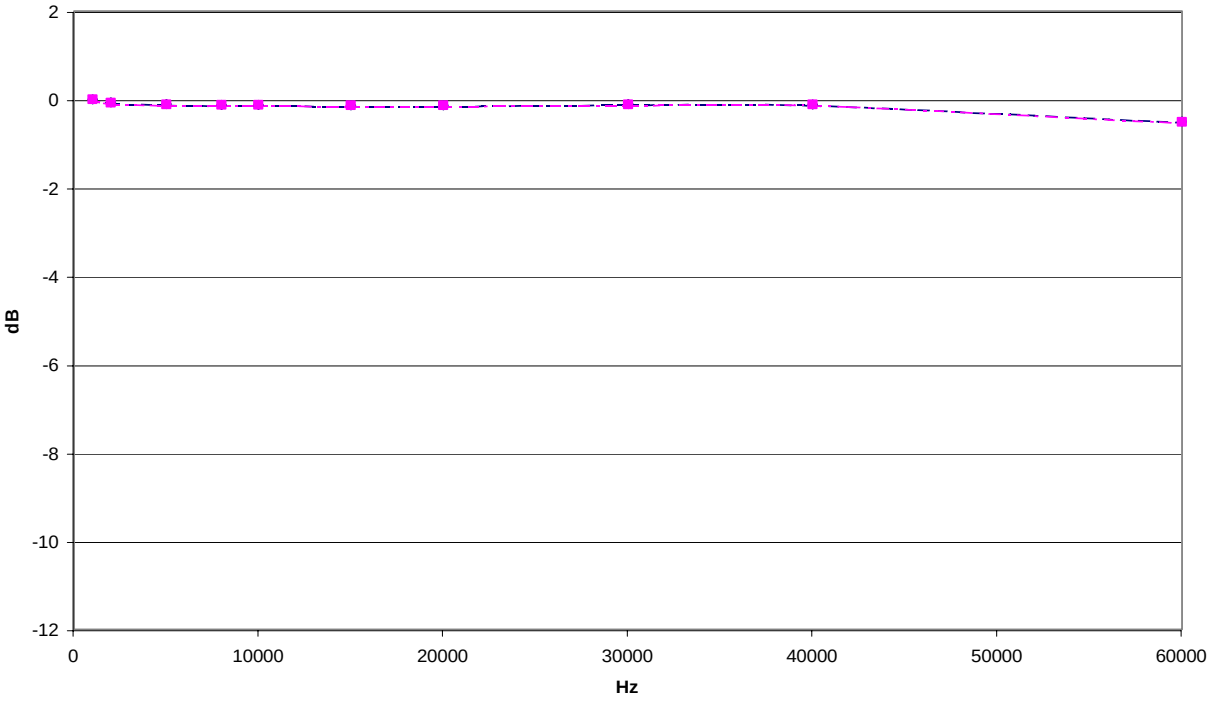


Figure 9. Audio Bandwidth Measurements (0 to 60 kHz) Without Pre-Emphasis

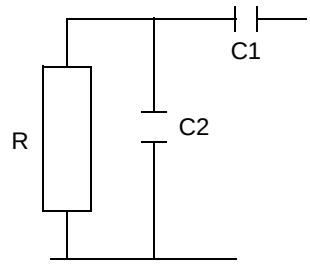


Figure 10. PLL Loop Filter

Loop filter equation: $\omega o = \sqrt{\frac{Kpd \times Kosc}{N \times C1}}$, $Q = \frac{1}{R \times C1 \times \omega o}$, with

- ωo = 3-dB cutoff frequency
- *Kpd* = 1-µA phase detector current
- *Kosc* = 5 MHz/V sound oscillator slope. (In fact, *Kosc* = 40 MHz/prescaler divider = 8.) This provides 5 MHz/V.
- *N* = Sound divider ratio
- *Q* = quality factorvR

C2, added to minimize glitches, is usually set to one tenth the size of C1. For example:

- Fref = 31.25 kHz $\rightarrow$ *N* = 5.5 MHz / 31.25 kHz = 176

  Assuming *C*1 = 1 µF, then ωo = 168 rad, and Fo = 27 Hz

Q depends on the desired frequency response. Choosing Q = 0.7 as a starting point, then R = 8.5 KΩ. The resistance acts directly on the factor quality and can be adjusted to create a peak on the low-frequency range. It is recommended that the value of R be adjusted experimentally depending on the application and requirements.

16 High Speed I^{2}C Compatible Bus

16.1 Specification Conditions

Each of the characteristics listed in Table 27 and Table 28 is classified as one of the following types:

- A—100% tested
- B—100% correlation tested
- C—Characterized on samples
- D—Design parameter

See Section 14, “Characterization Measurement Conditions,” for each C-type parameter.

Unless otherwise specified, V_{CC} = 5.0 V, TA = 25°C.

Table 27. Electrical Characteristics

Electrical Characteristics	Symbol	Minimum	Typical	Maximum	Unit	Type
SDA/SCL output current at 0V		–5	–2	—	µA	A
SDA/SCL low input level	V_{IL}	—	—	1.5	V	B
SDA/SCL high input level	V_{IH}	2.1	—	—	V	B
SDA/SCL input current for input level from 0.4 V to 0.3 V_{CC}		–5	—	5	µA	C
SDA/SCL input level		0	—	V_{CC}+0.3	V	D
SDA/SCL capacitance		—	—	10	pF	C
ACK low output level (3 mA sinking current)		—	—	0.3	V	C
ACK low output level (9 mA sinking current)		—	—	0.8	V	C

Table 28. Timing Characteristics

Timing Characteristics	Symbol	Minimum	Typical	Maximum	Unit	Type
Bus clock frequency		0	—	800	kHz	C
Bus free time between stop and start	T_{buf}	200	—	—	ns	C
Setup time for start condition	$T_{su;sta}$	500	—	—	ns	C
Hold time for start condition	$T_{hd;sta}$	500	—	—	ns	C
Data setup time	$T_{su;dat}$	0	—	—	ns	C
Data hold time	$T_{hd;dat}$	0	—	—	ns	C
Setup time for stop condition	$T_{su;sto}$	500	—	—	ns	C
Hold time for stop condition	$T_{hd;sto}$	500	—	—	ns	C
Acknowledge propagation delay	$T_{ack;low}$	—	—	300	ns	C
SDA fall time at 3 ma sink I and 130-pF load		—	—	50	ns	C
SDA fall time at 3 ma sink I and 400-pF load		—	—	80	ns	C
SDA rise time SCL fall/rise time		— —	— —	300 300	ns ns	C C
Pulse width of spikes suppressed by the input filter		—	—	50	ns	C

16.2 Timing Definitions

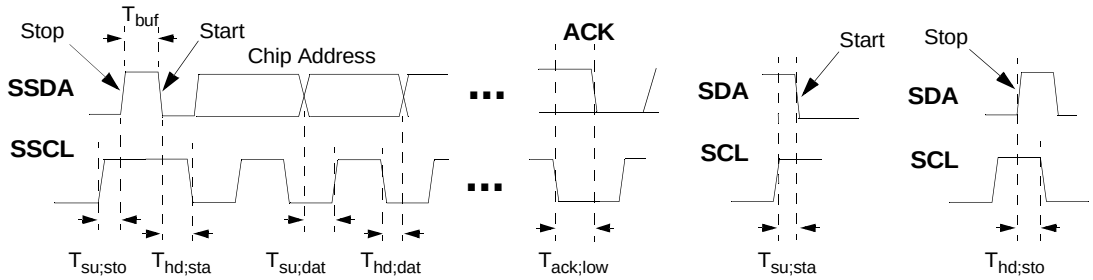


Figure 11. SSDA/SSCL Timing

16.3 Level Definitions

SDA/SCL high and low levels are designed to be compatible with 0–5 V and 0–3.3 V SDA/SCL signals.

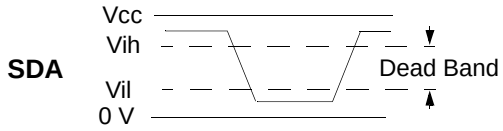


Figure 12. SDA/SCL Levels

16.4 High-Speed I²C-Compatible Bus Format

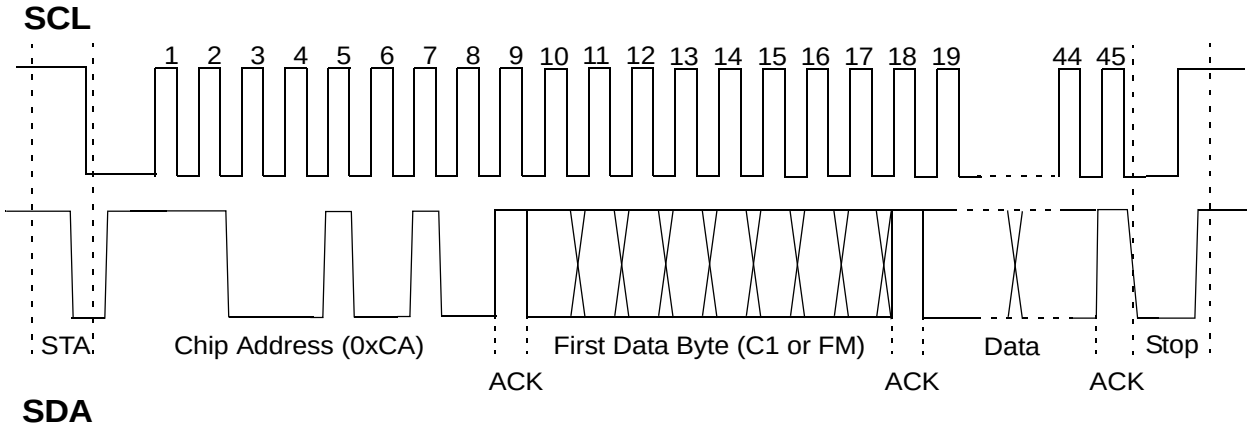


Figure 13. I²C Bus Timing

16.5 I²C Write-Mode Format and Bus Receiver

NOTE

The information in this section concerning I²C address selection applies to the 20-pin package only. The I²C address in the 16-pin packages is set at 0xCA and cannot be changed.

It is possible to select one specific I²C address from among four available addresses. This selection is controlled by an external pin (CAS) where an external resistor is connected to ground. By changing the value of this resistor it is possible to change the DC level on the multi-level CAS pin. This DC level is compared against internal thresholds (1.65, 0.42 and 2.82 V) and, depending on the result, one of the available addresses is selected according to Table 29.

When chip addresses CC or C8 are selected, the DC level at the CAS pin is set by a ratio of an external resistor (33 KΩ or 180 KΩ ±10%) and the internal pull-up resistor (85 KΩ typical with a tolerance of 40% worst case).

Table 29. Chip Address Selected Versus CAS Pin Level

External Resistor on Pin CAS	I²C address
Open	0xCA
180-KΩ pull-down	0xC8
33-KΩ pull-down	0xCC
0 (connected to ground)	0xCE

The bus receiver operates the I^2C-compatible data format. The chip address (I^2C bus) is shown in Table 30.

Table 30. Chip Address (I^2C Write Mode)

1 1 0 0 1 0 0 0 (ACK) = 0xC8 in write mode
1 1 0 0 1 0 1 0 (ACK) = 0xCA in write mode
1 1 0 0 1 1 0 0 (ACK) = 0xCC in write mode
1 1 0 0 1 1 1 0 (ACK) = 0xCE in write mode

In write mode, each ninth data bit (bits 9, 18, 27, 36, and 45) is an acknowledge bit (ACK) during which the MCU sends a logic 1 and the modulator circuit answers on the data line by pulling it low. Besides the chip address, the circuit needs 2 or 4 data bytes for operation. The sequences of data bytes shown in Table 31 are the permitted incoming information.

Table 31. Permitted Data Bytes (Incoming Information)

Example 1	STA	CA	C1	C0	STO		
Example 2	STA	CA	FM	FL	STO		
Example 3	STA	CA	C1	C0	FM	FL	STO
Example 4	STA	CA	FM	FL	C1	C0	STO

Notes:

- STA = Start condition
- FM = Frequency information, high order bits
- C1 = Control information, high order bits
- STO = Stop condition
- CA = Chip Address
- FL = Frequency information, low order bits
- CO = Control information, low order bits

After the chip address (CA), 2 or 4 data bytes may be received.

- If 3 data bytes are received, the third one is ignored.
- If 5 or more data bytes are received, the fifth and following ones are ignored, and the last ACK pulse is sent at the end of the fourth data byte.

The first and third data bytes contain a function bit, which lets the IC distinguish between frequency information and control information. If the function bit is a logic 1, the two following bytes contain control information. The first data byte after the chip address may be byte CO or byte FM. The 2 bytes of frequency information are preceded by a logic 0.

16.6 I^2C Read Mode Format

The chip address (I^2C bus) is shown in Table 32.

Table 32. Chip Address (I^2C Read Mode)

1 1 0 0 1 0 0 1 (ACK) = 0xC9 (hex) in read mode
1 1 0 0 1 0 1 1 (ACK) = 0xCB (hex) in read mode
1 1 0 0 1 1 0 1 (ACK) = 0xCD (hex) in read mode
1 1 0 0 1 1 1 1 (ACK) = 0xCF (hex) in read mode

The incoming information consists of the read-mode chip address byte. The device then answers with an ACK followed by 1 byte containing 3 bits of status information. No acknowledge is answered by the modulator after this byte.

17 Pin Circuit Schematics

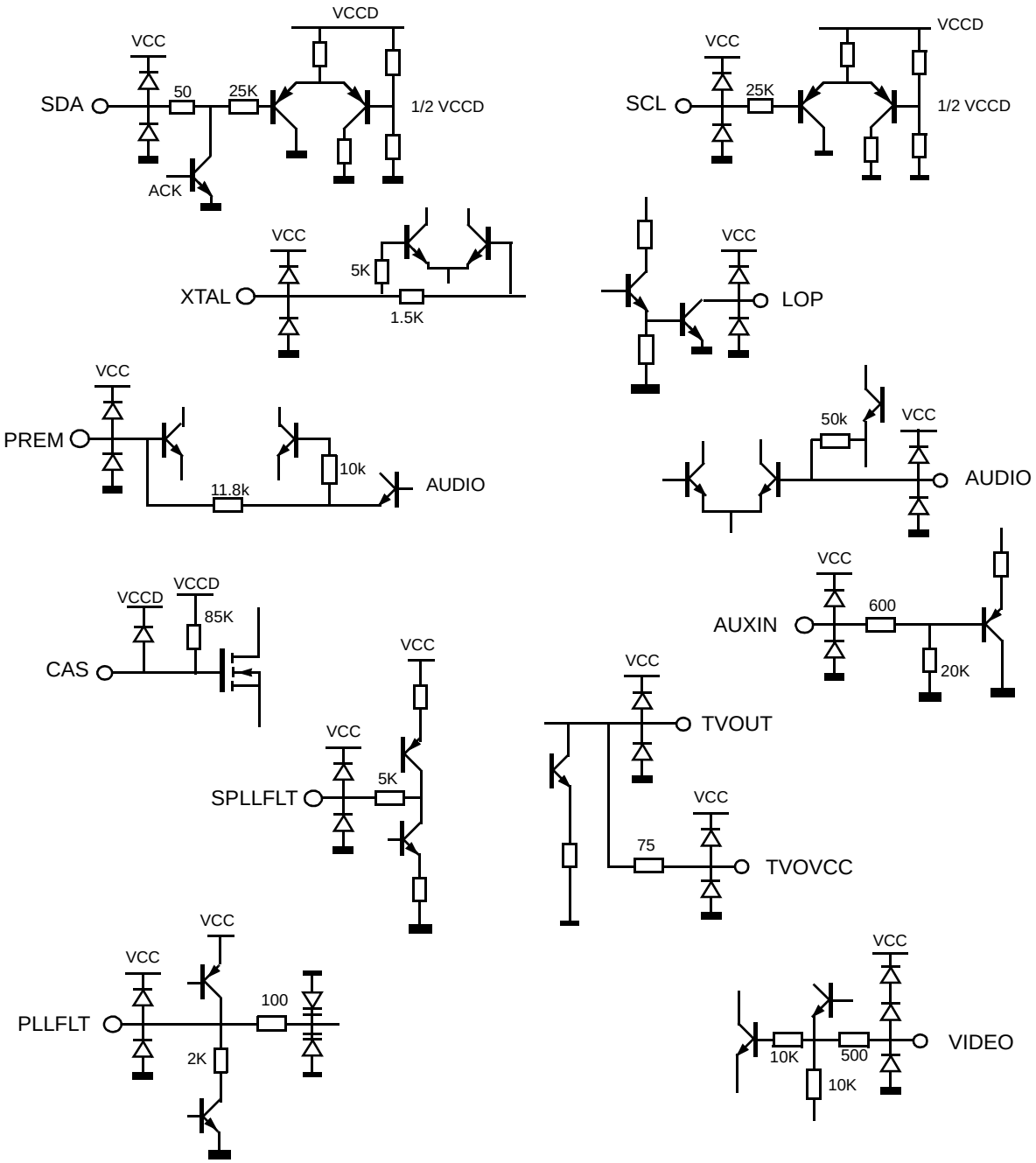


Figure 14. Pin Circuit Schematics

18 Application Diagrams

18.1 BiCMOS Modulator SO16NB Mono Application

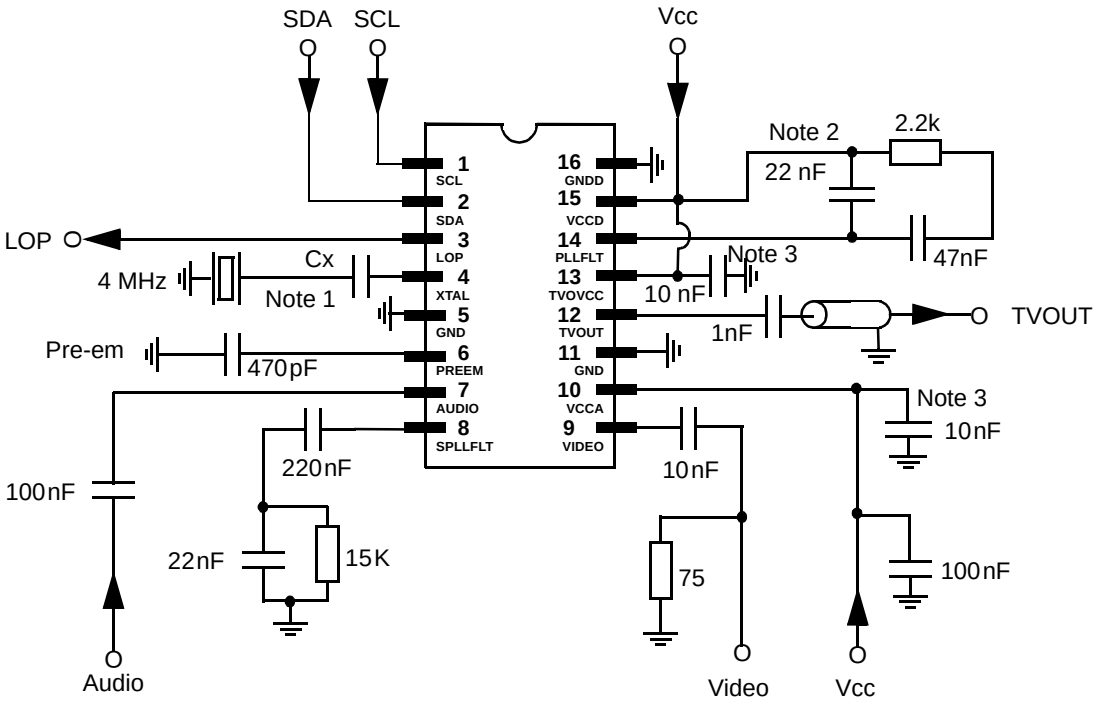


Figure 15. Proposed SO16 Package (Mono Application Schematic)

Notes:

1. Cx value depends on crystal characteristics. Cx = 27 pF on Motorola application board.
2. RF PLL loop filter components at pin 14 must be as close as possible to VCCD at pin 15.
3. Supply voltage decoupling capacitors must be as close as possible to ground.

18.2 BiCMOS Modulator SO16NB Stereo Application

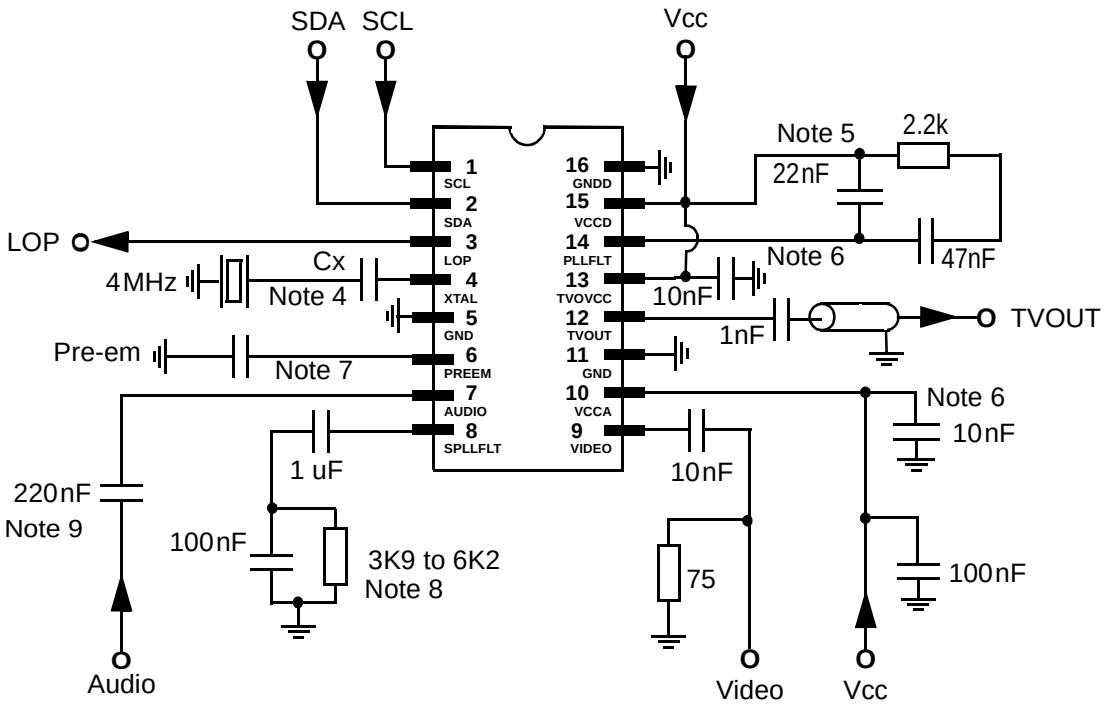


Figure 16. Proposed SO16 Package (Stereo Application Schematic)

Notes:

4. Cx value depends on crystal characteristics; Cx = 27 pF on Motorola application board.
5. RF PLL loop filter components at pin 14 must be as close as possible to FCC at pin 15.
6. Supply voltage decoupling capacitors must be as close as possible to ground.
7. For a stereo application, the audio signal is already encoded in the baseband stereo encoder. It is not necessary to create a pre-emphasis and in this case the pre-emphasis capacitor has to be removed. Sometimes for the same application it is useful to increase the FM deviation. To increase FM deviation, replace the original pre-emphasis capacitor with a 100-nF capacitor. Adding this kind of value boosts the deviation and does not create a pre-emphasis.
8. It is possible to create a peak for the low frequencies (from 30 to 80 Hz) by adjusting the resistor of the sound loop filter. A flat response is given with a value of 5.6 KΩ but this value can be set to 4.7 KΩ. This gives a peak of about 1 dB at 40 Hz and extends the low-frequency cut-off at 28 Hz. The value of the audio input series capacitor has been increased in order to have a lower cut-off frequency.
9. The value of the audio input series capacitor has been increased in order to have a lower cutoff frequency.

18.3 BiCMOS Modulator QFN20 Mono Application

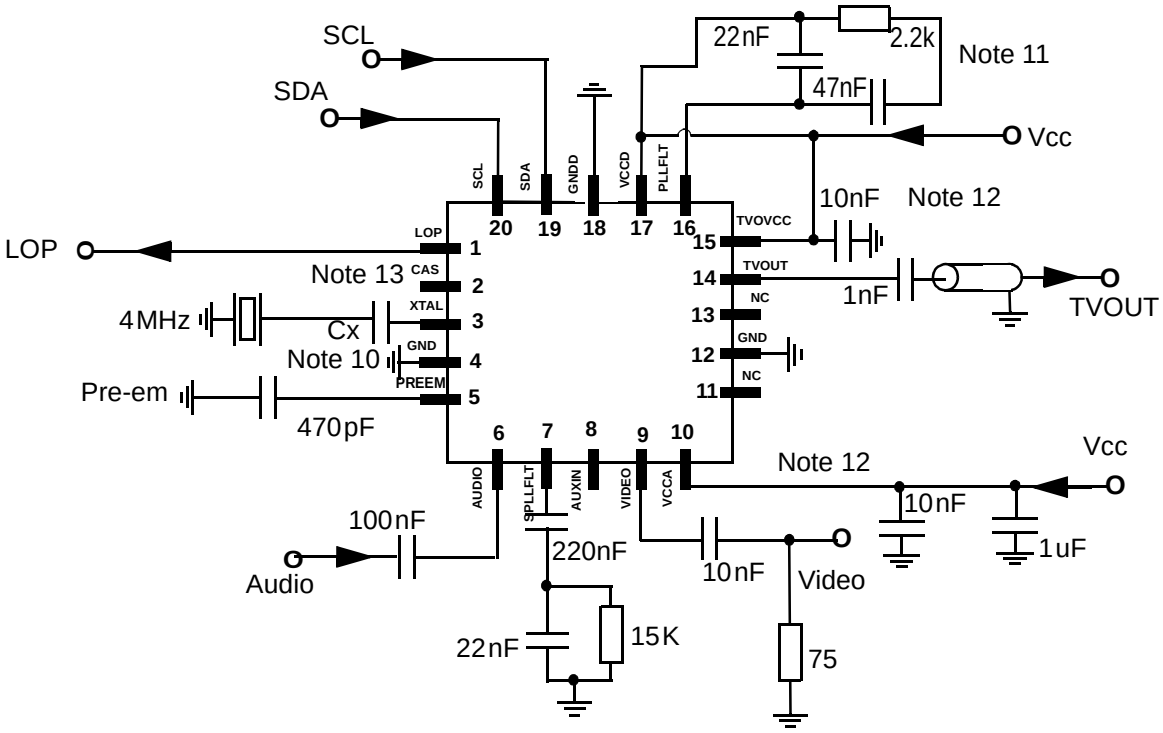


Figure 17. Proposed QFN20 Package (Mono Application Schematic)

Notes:

10. Cx value depends on crystal characteristics; Cx = 27 pF on Motorola application board
11. RF PLL loop filter components at pin 16 must be as close as possible to FCC at pin 17.
12. Supply voltage decoupling capacitors must be as close as possible to ground.
13. Chip address select pin open (default I^2C address = 0xCA).

18.4 BiCMOS Modulator QFN20 Stereo Application

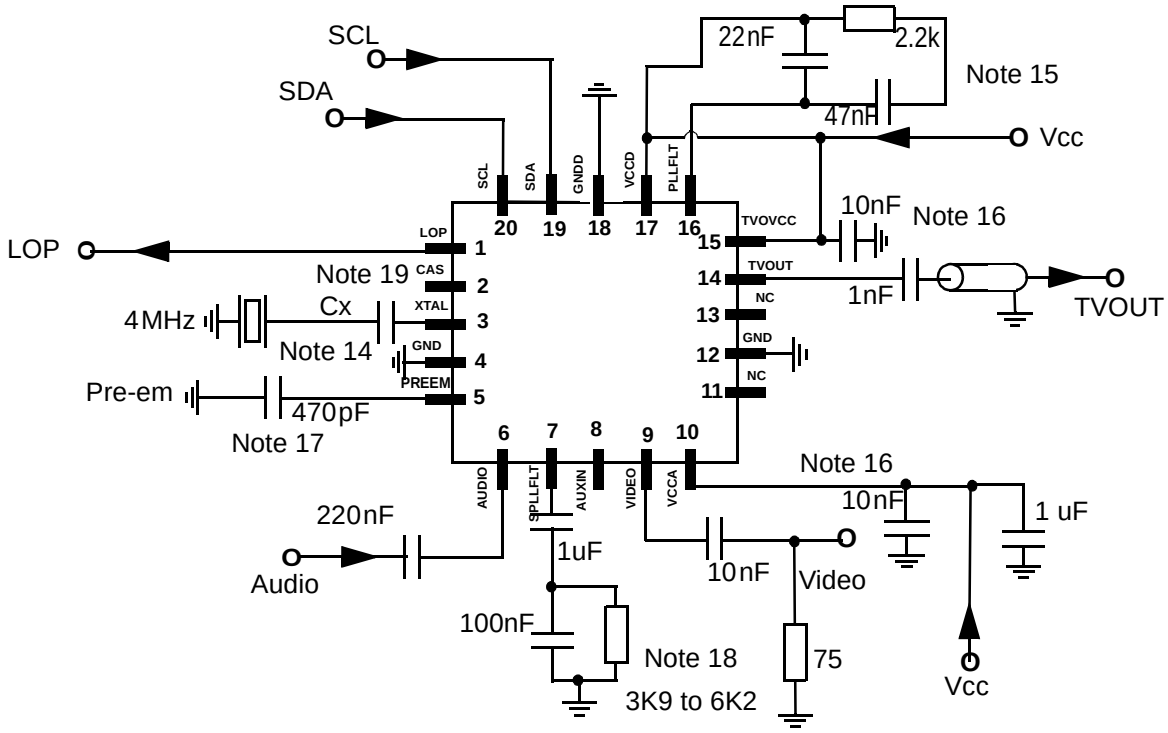


Figure 18. Proposed QFN20 Package (Stereo Application Schematic)

Notes:

14. Cx value depends on crystal characteristics; Cx = 27 pF on Motorola application board.
15. RF PLL loop filter components at pin 16 must be as close as possible to FCC at pin 17.
16. Supply voltage decoupling capacitors must be as close as possible to ground.
17. For a stereo application, the audio signal is already encoded in the baseband stereo encoder. It is not necessary to create a pre-emphasis and in this case the pre-emphasis capacitor has to be removed. Sometimes for the same application it is useful to increase the FM deviation by replacing the original pre-emphasis capacitor with a 100-nF capacitor. Adding this value boosts the deviation and does not create a pre-emphasis.
18. It is possible to create a peak for the low frequencies (from 30 to 80 Hz) by adjusting the sound loop filter resistor. A flat response is given with a value of 5.6 KΩ but this value can be set to 4.7 KΩ. This gives a peak of about 1 dB at 40 Hz and extends the low-frequency cut-off at 28 Hz (see audio section).
19. Chip address select pin open (default I^2C address = 0xCA)
    The value of the audio input series capacitor has been increased in order to have a lower cut-off frequency.

19 MC44BS373CA Evaluation Board Schematic and Layout

19.1 SO16NB Board PCB Layout

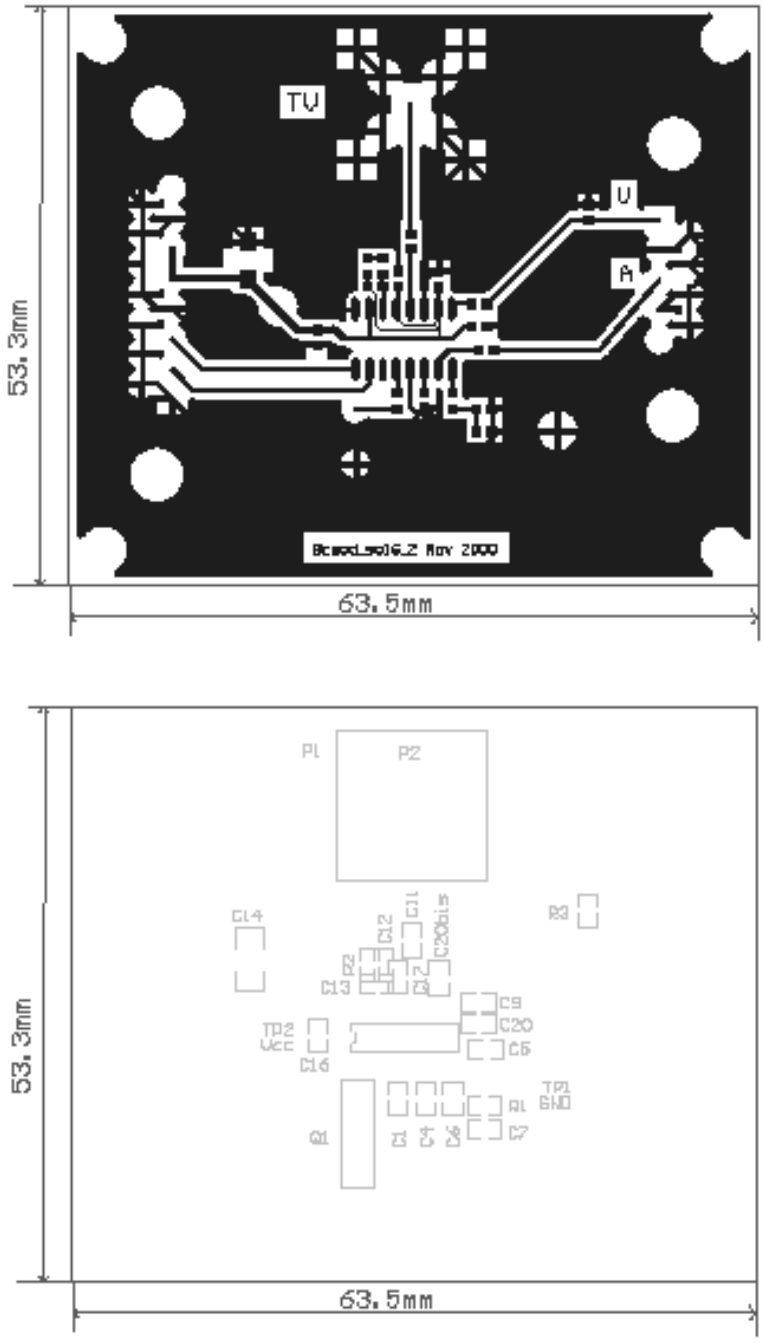


Figure 19. Evaluation Board PCB Layout (SO16NB Package)

19.2 SO16NB Board Schematic

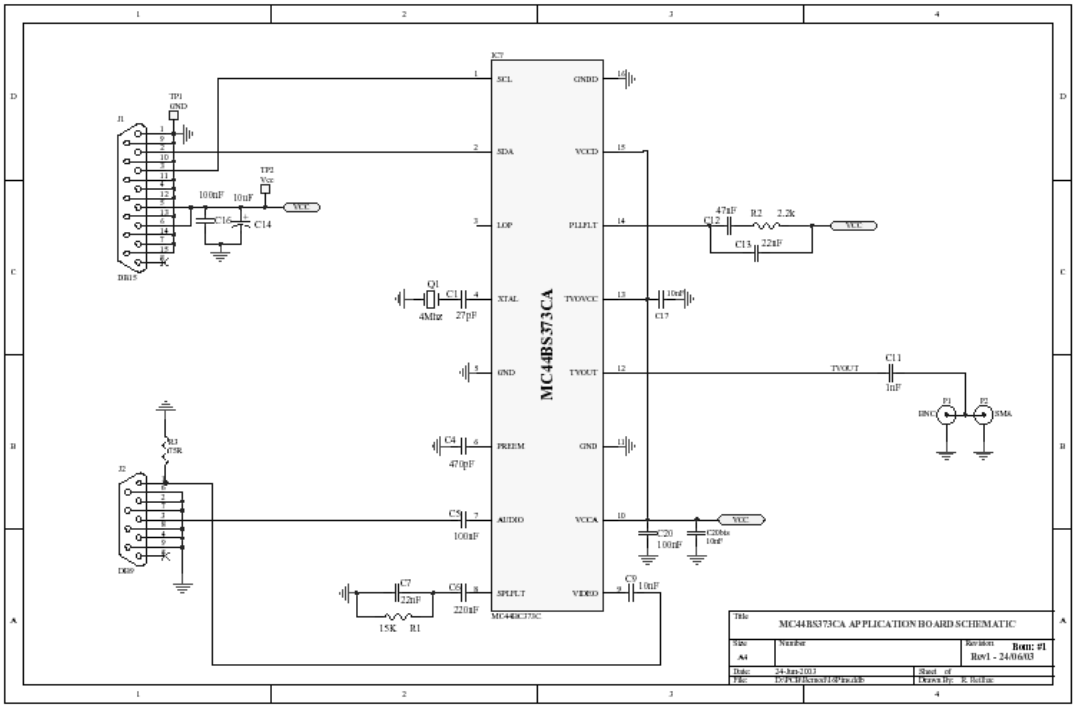
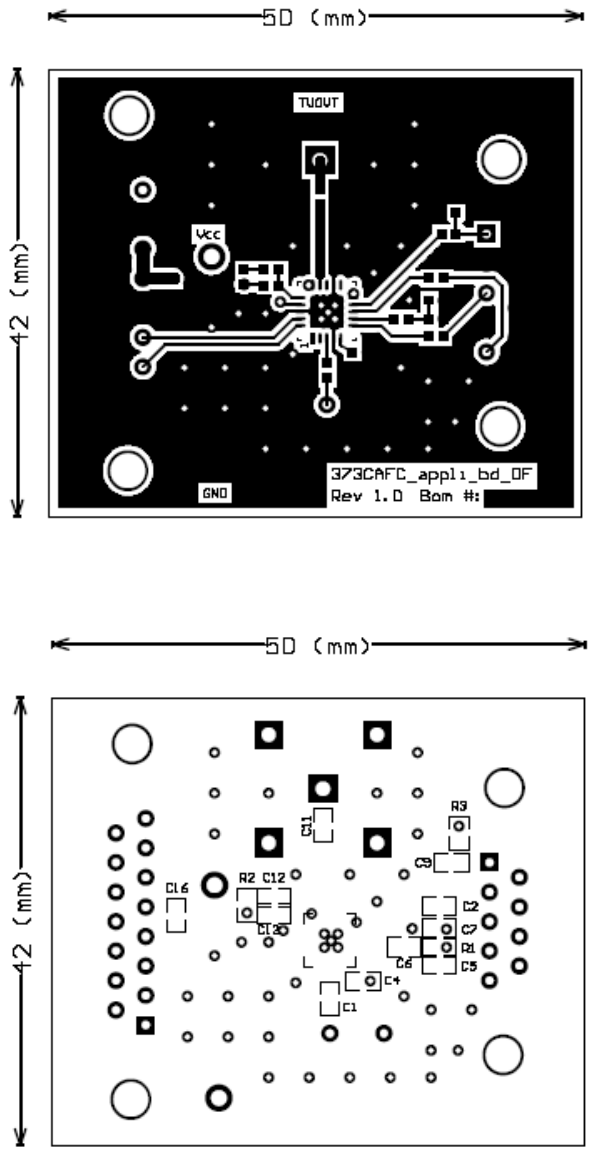


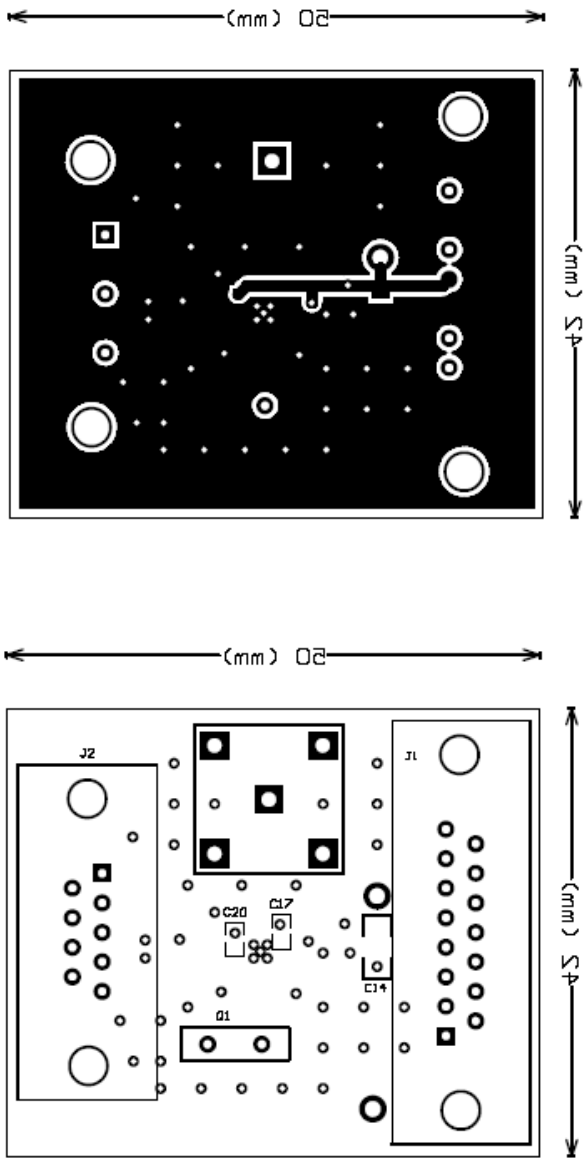
Figure 20. Evaluation Board Schematic (SO16NB Package)

19.3 QFN20 Board PCB Layout



Top Layer

Figure 21. Evaluation Board PCB Layout (QFN20 Package)



Bottom Layer

Figure 22. Evaluation Board PCB Layout (QFN20 Package)

19.4 QFN20 Board Schematic

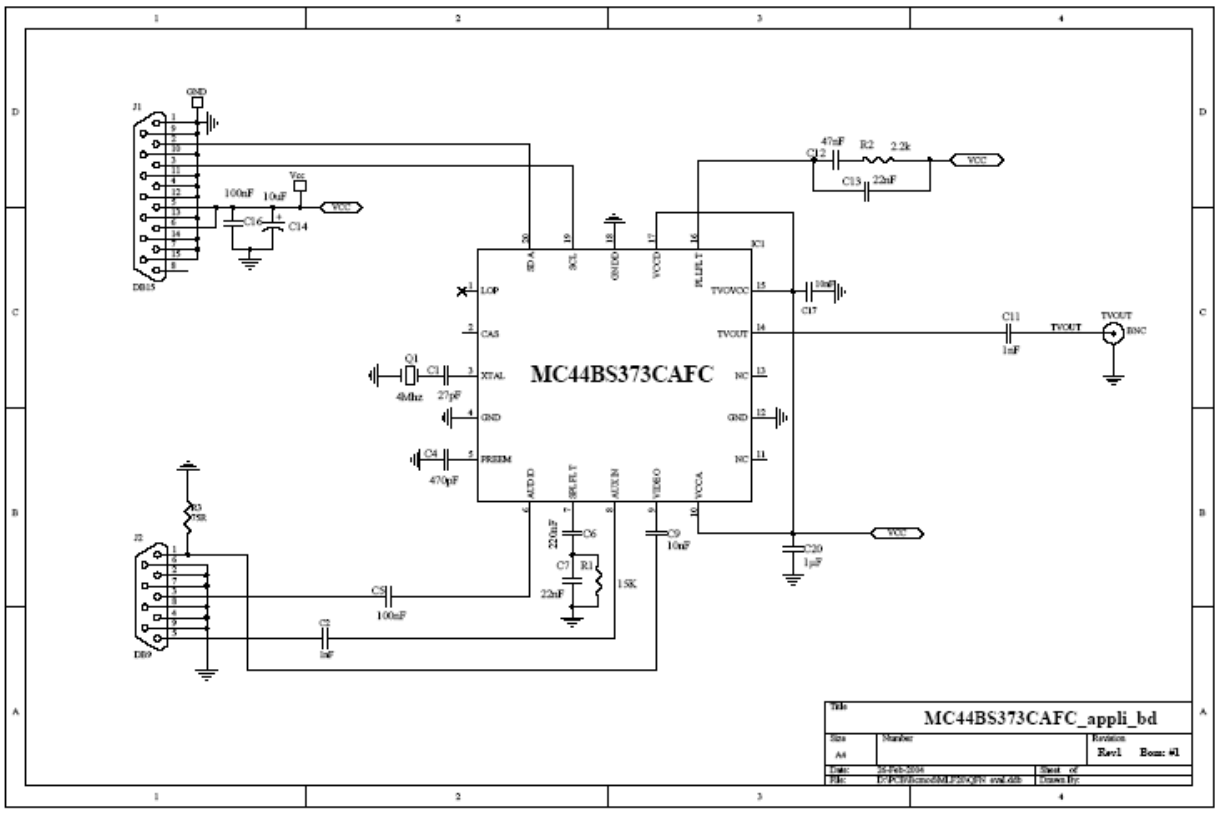


Figure 23. Evaluation Board Schematic (QFN20 Package)

20 Packaging Instructions

Tape and reel packaging is per 12MRH00360A issue Y with the following conditions applicable for dual in-line SOP (SOIC) package and quad flat pack no lead square (QFN).

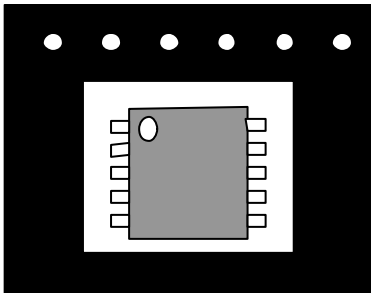


Figure 24. Dual In-line SOP (SOIC)

Component orientation: Arrange parts with the pin-1 side closest to the tape's round sprocket holes on the tape's trailing edge.

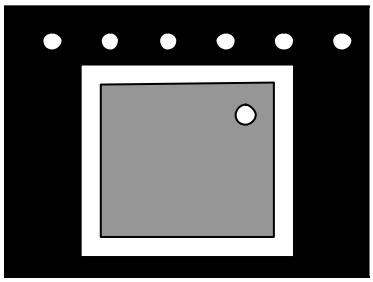


Figure 25. Quad Flat Pack No Lead Square

Moisture sensitivity levels are as follows:

- MC44BS373CAD,R2—Moisture sensitivity level 1, no dry pack required
- MC44BS373CAFC,R2 lead free packages—Moisture sensitivity level 3, dry pack required
- MC44BS373CAEF,R2 lead free packages—Moisture sensitivity level 3, dry pack required

21 Marking Instructions

21.1 SO16 NB Marking

Bar marked part way across pin 1 end of package. Bar width 10 to 20 mils, length to be at least four times bar width. Bar placement may extend across chamfer and dimple areas.



- 1st line:
  M44BS373CA (Part number coded on 10 digits)
- 2nd line:
  Assembly site code **AW** (2 digits) followed by the
  wafer lot code **L** (1 digit),
  year **Y** (1 digit) and
  work week **WW** (2 digits)

21.2 SO16 NB Lead Free Marking

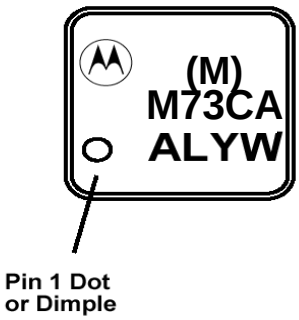
Bar marked part way across pin 1 end of package. Bar width 10 to 20 mils, length to be at least four times bar width. Bar placement may extend across chamfer and dimple areas.



- 1st line:
  M44BS373CA (Part number coded on 10 digits)
- 2nd line:
  Assembly site code **AW** (2 digits) followed by the
  wafer lot code **L** (1 digit),
  year **Y** (1 digit) and
  work week **WW** (2 digits)

21.3 QFN20 Marking

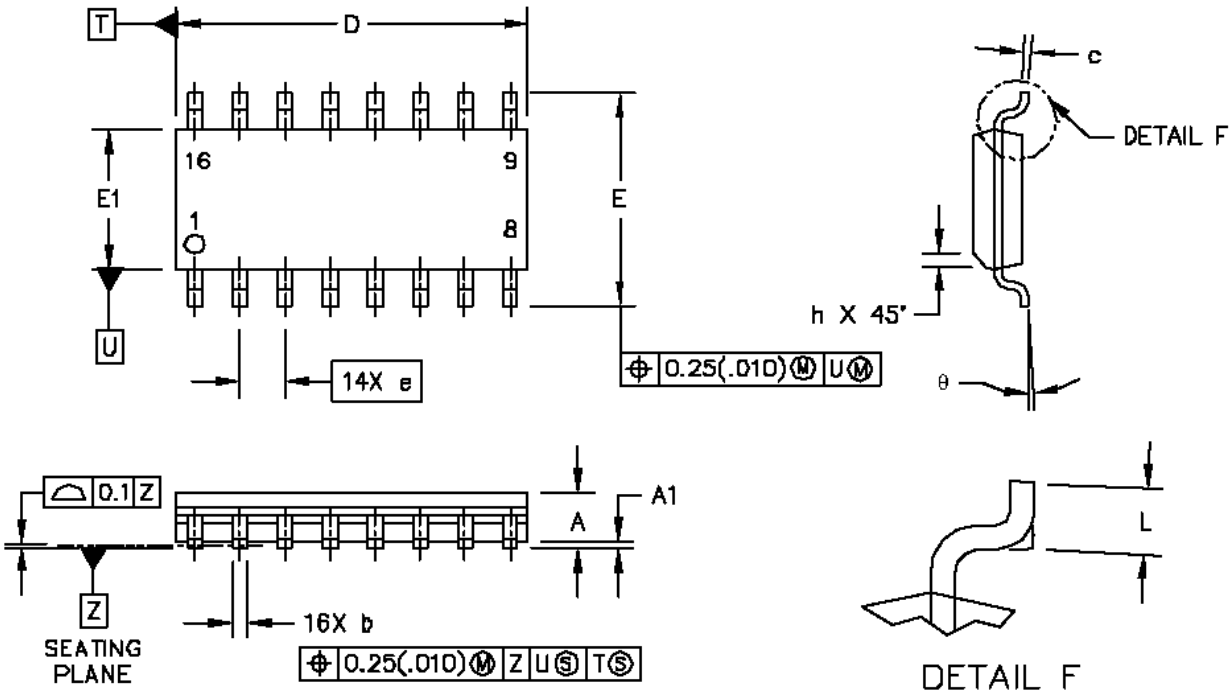
Compliant with 12MRH00191A specification for package code 126.



- 1st line: **M73CA**
  (Part number coded on 4 digits)
- 2nd line: **ALYW**
  (Assembly site code **A** (1 digit)
  wafer lot code **L** (1 digit),
  year **Y** (1 digit) and
  work week **W** (1 digit)

22 Case Outlines

22.1 SO16 Case



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.054	0.068
A1	0.1	0.25	0.004	0.009
D	9.8	10	0.385	0.393
E	5.8	6.2	0.229	0.244
E1	3.8	4	0.150	0.157
b	0.35	0.49	0.014	0.019
c	0.19	0.25	0.008	0.009
e	1.27 BSC		0.050 BSC	
L	0.4	1.25	0.016	0.049
h	0.25	0.5	0.010	0.019
Q	0^o	7^o	0^o	7^o

Note: 1. Dimensions and Tolerances per ASME Y14.5M, 1994.

Note: 2. Controlling dimension: Millimeters.

Note: 3. Dimensions D and E1 do not include mold protrusion.

Note: 4. Maximum mold protrusion 0.15 (0.006) per side.

Note: 5. Dimension b does not include Dambar protrusion.
Allowable Dambar protrusion shall be 0.127 (0.005) total in excess of the b dimension at maximum material condition.

Figure 26. SO16NB Package

22.2 QFN20 Case

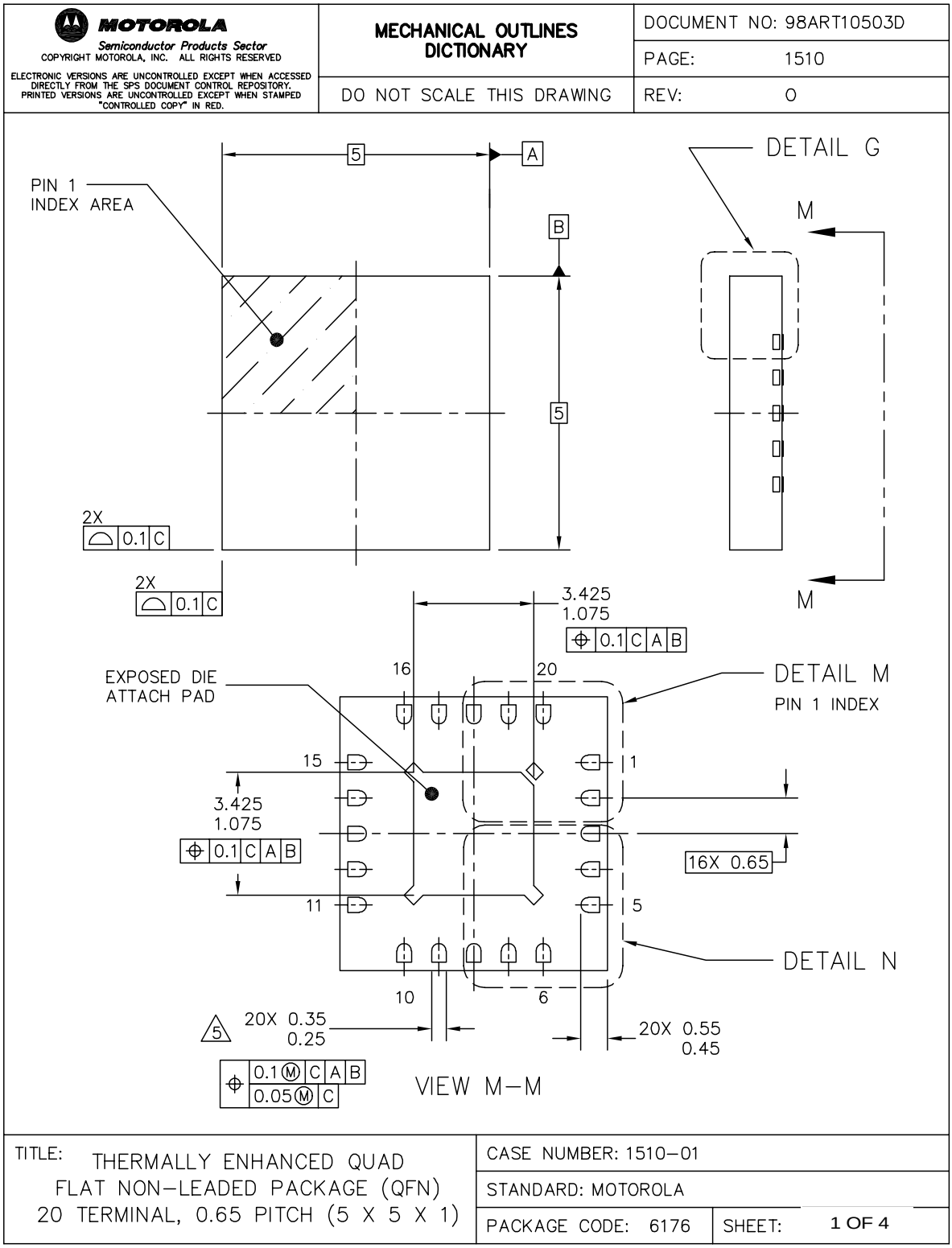


Figure 27. QFN20 Package (1 of 4)

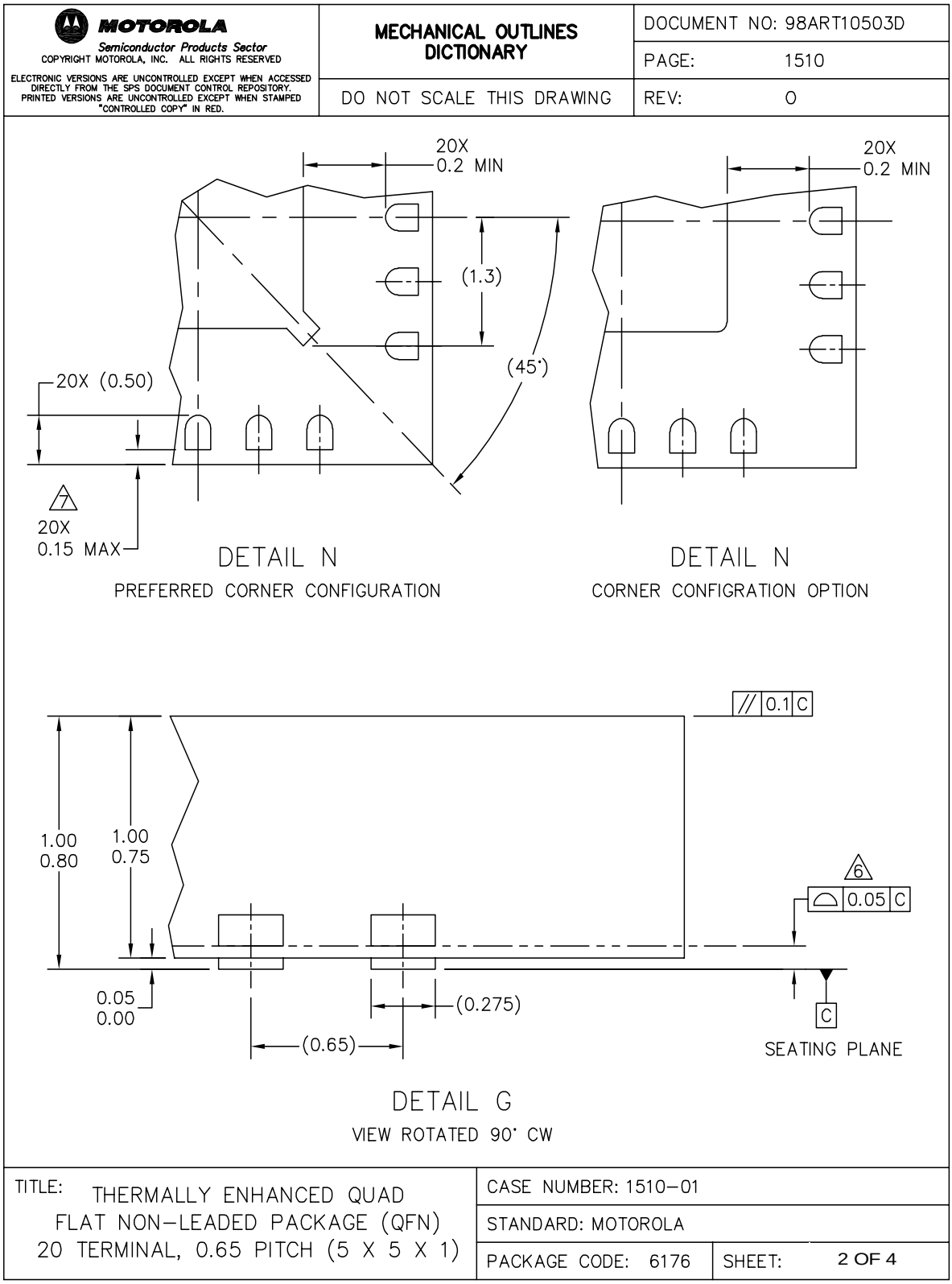


Figure 28. QFN20 Package (2 of 4)

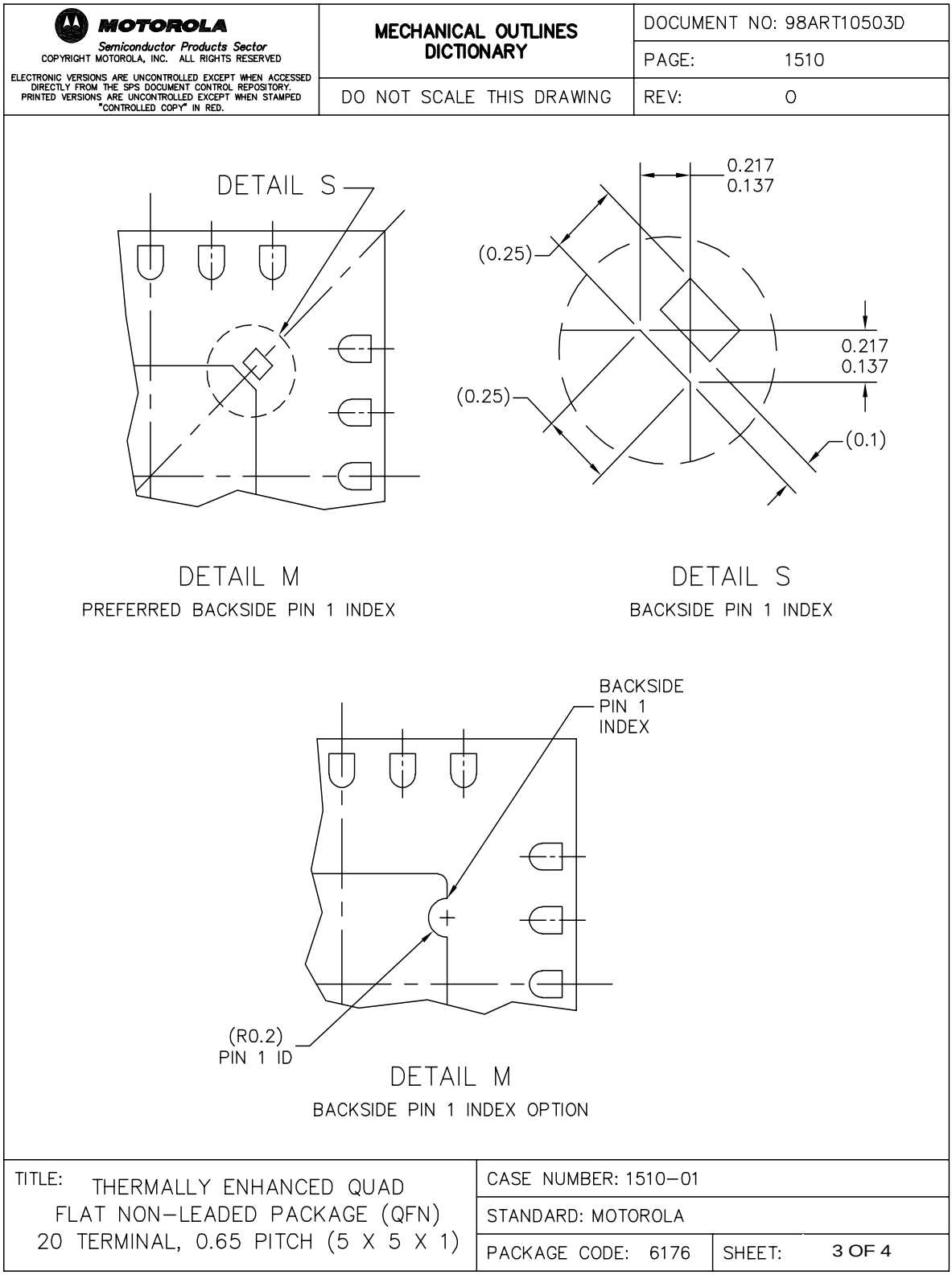


Figure 29. QFN20 Package (3 of 4)

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		PAGE: 1510
	DO NOT SCALE THIS DRAWING	REV: O

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM PACKAGE WARPAGE IS 0.05 mm.
4. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
5. THIS DIMENSION APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 mm AND 0.30 mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL. THIS DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
6. COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.
7. A MAXIMUM 0.15 mm LEAD RECESSION MAYBE PRESENT LEAD LENGTH MINUS LEAD RECESSION TO BE EQUAL TO OR GREATER THAN 0.30 mm.
8. FOR ANVIL SINGULATED QFN PACKAGES, MAXIMUM DRAFT ANGLE IS 12°.

TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 20 TERMINAL, 0.65 PITCH (5 X 5 X 1)	CASE NUMBER: 1510–01	
	STANDARD: MOTOROLA	
	PACKAGE CODE: 6176	SHEET: 4 OF 4

Figure 30. QFN20 Package (4 of 4)

23 Document Revision History

Table 33 provides a revision history for this data sheet.

Table 33. Document Revision History

Rev. No.	Date	Substantive Change(s)
2.5	05/14/2004	Non-technical edits Tables reformatted Added note nine to Figure 16
2.6	05/26/2004	Corrected resistor values from 56 KΩ to 5.6 KΩ and from 47 KΩ to 4.7 KΩ in: • Notes to Figure 16 and Figure 18 • Section 15.11, “Sound Section” Corrected capacitor labeling in Figure 10 Corrected settings for picture-to-sound ratio in Table 22 (PS bit settings were reversed) Added label for note 17 on Figure 18
	06/16/2004	Removed pin numbers from Figure 2 Removed warnings from Figure 15, Figure 16, Figure 17, and Figure 18 Corrected spelling of pin SPLLFLT (was SPLFLT) Changed operating temperature range from 0–70 to –20–85. Added note to section 16 stressing that I^2C address selection is not available for the 16-pin packages

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