JFET-INPUT DUAL OPERATIONAL AMPLIFIERS

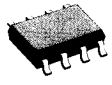
- HIGH SLEW-RATE ... 13 V/μs TYP.
- LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW INPUT BIAS AND OFFSET CURRENTS
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE ... JFET-INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH-UP-FREE OPERATION

The TL082 JFET-input operational amplifiers are designed to offer high slew-rate, low input bias and offset current, and low offset voltage temperature coefficient. Each JFET-input operational amplifier incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.

Devices with an "I" suffix are characterized for operation from -25°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C. The "M" devices are characterized for operation from -55 to 125°C.



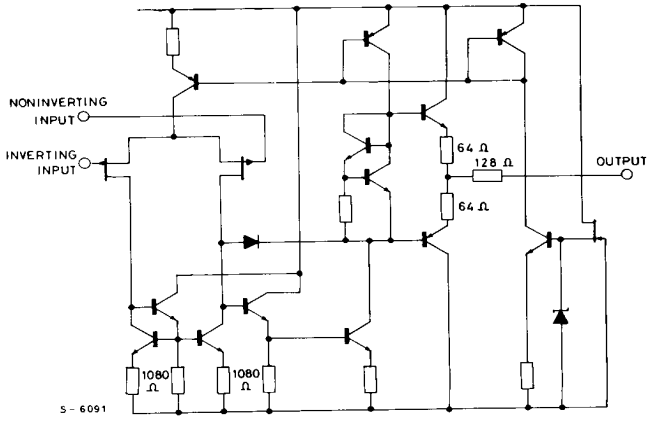
Minidip (Plastic and Ceramic)



SO-8

SCHEMATIC DIAGRAM

(one section)



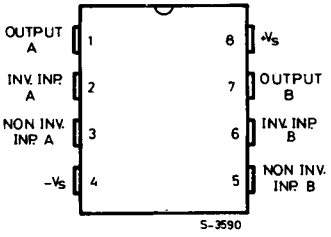
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ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage		± 18	V
V_{is}	Differential input voltage		± 30	V
V_i	Input voltage		± 15	V
T_{op}	Operating temperature	(TL082I)	-25 to 85	°C
		(TL082C)	0 to 70	°C
		(TL082M)	-55 to 125	°C
T_j	Junction temperature		150	°C
T_{stg}	Storage temperature		-65 to 150	°C

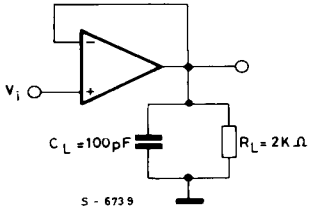
CONNECTION DIAGRAM AND ORDERING NUMBERS

(Top view)

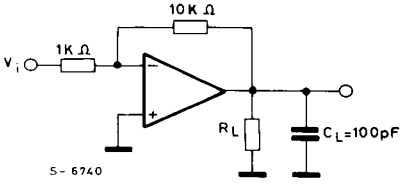


0 to 70°C	-25 to 85°C	-55 to 125°C	Package
TL082CJG TL082ACJG TL082BCJG	TL082IJG — —	TL082MJG — —	Ceramic Minidip
TL082CP TL082ACP TL082BCP	TL082IP — —	— — —	Plastic Minidip
TL082CD	TL082ID	—	SO-8

TEST CIRCUITS



Unity gain amplifier



Gain of 10 inverting amplifier

THERMAL DATA

			Plastic Minidip	Ceramic Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	120°C/W	150°C/W	200°C/W

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ELECTRICAL CHARACTERISTICS ($V_s = \pm 15V$, $T_{amb} = 25°C$, otherwise specified)

Parameter	Test Conditions		"I"			"C"			"M"			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS} Input offset voltage	$R_s = 50\Omega$	TL082		3	6		5	15		3	6	mV
		TL082A					3	6				
		TL082B					2	3				
	$R_s = 50\Omega$, T_{amb} = full range	TL082			9			20			9	
		TL082A						7.5				
		TL082B						5				
$\frac{\Delta V_{OS}}{\Delta T}$ Input offset voltage drift	$R_s = 50\Omega$, T_{amb} = full range			10			10			10		$\mu V/°C$
I_{OS} Input offset current		TL082		5	100		5	200		5	100	pA
		TL082A					5	100				
		TL082B					5	100				
	T_{amb} = full range	TL082			10			5			20	nA
		TL082A						3				
		TL082B						3				
I_b Input bias current		TL082		30	200		30	400		30	200	pA
		TL082A					30	200				
		TL082B					30	200				
	T_{amb} = full range	TL082			20			10			50	nA
		TL082A						7				
		TL082B						7				
V_{CM} Common mode input voltage range		TL082	± 11	± 12		± 10	± 11		± 11	± 12		V
		TL082A				± 11	± 12					
		TL082B				± 11	± 12					
V_{OPP} Large signal voltage swing		$R_L = 10K\Omega$	24	27		24	27		24	27		V
	T_{amb} = full range	$R_L \geq 10K\Omega$	24			24			24			
		$R_L \geq 2K\Omega$	20	24		20	24		20	24		
G_V Large signal voltage gain	$R_L \geq 2K\Omega$, $V_o = \pm 10V$	TL082	50	200		25	200					V/mV
		TL082A				50	200					
		TL082B				50	200					
	$R_L \geq 2K\Omega$, $V_o = \pm 10V$, T_{amb} = full range	TL082	25			15			15			
		TL082A				25						
		TL082B				25						
B Unity gain bandwidth				3			3			3		MHz
R_i Input resistance				10^{12}			10^{12}			10^{12}		Ω
CMR Common mode	$R_s \geq 10K\Omega$	TL082	80	86		70	76		80	86		
		TL082A				80	86					
		TL082B				80	86					
SVR Supply voltage	$R_s \geq 10K\Omega$	TL082	80	86		70	76		80	86		dB
		TL082A				80	86					
		TL082B				80	86					
I_S Supply current	$R_L = \infty$			2.8	5.6		2.8	5.6		2.8	5.6	mA

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ELECTRICAL CHARACTERISTICS (Continued)

Parameter		Test Conditions		"I"			"C"			"M"			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
CS	Channel separation	G_V = 100			120			120			120		dB
SR	Slew-rate at unity gain	V_I = 10V C_L = 100pF	R_L = 2KΩ		13			13		8	13		V/μs
t_r	Rise time	V_I = 20mV C_L = 100pF	R_L = 2KΩ		0.1			0.1			0.1		μs
	Overshot factor				10			10			10		%
e_N	Total input noise voltage	R_S = 100Ω f = 1KHz			25			25			25		$\frac{nV}{\sqrt{Hz}}$

Fig. 1 - Maximum peak to peak output voltage vs. frequency.

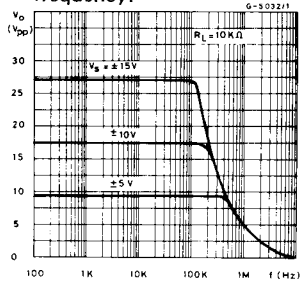


Fig. 2 - Maximum peak to peak output voltage vs. frequency.

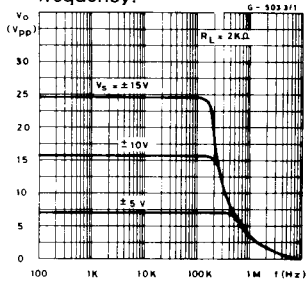


Fig. 3 - Maximum peak to peak output voltage vs. load resistance.

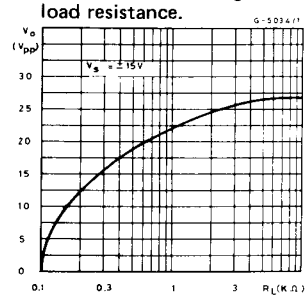


Fig. 4 - Large signal voltage gain and phase shift vs. frequency.

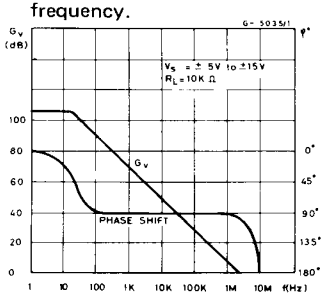


Fig. 5 - Supply current vs. temperature

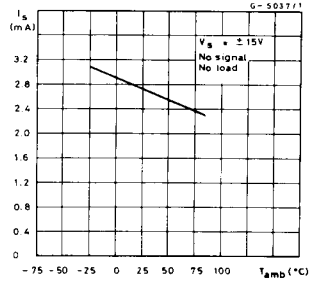
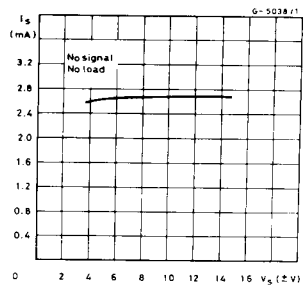


Fig. 6 - Supply current vs. supply voltage.



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Fig. 7 - Input bias current vs. temperature.

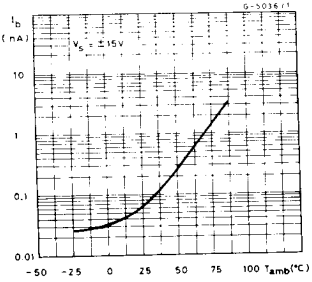


Fig. 8 - Voltage follower large signal pulse response

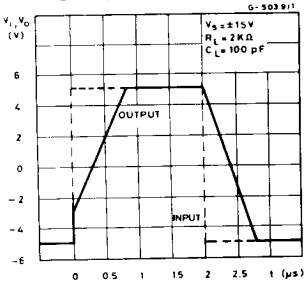


Fig. 9 - Output voltage vs. elapsed time.

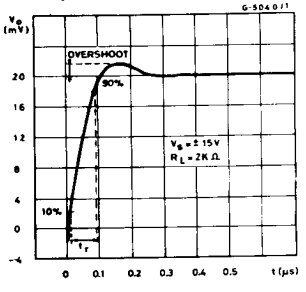


Fig. 10 - Equivalent input noise voltage vs. frequency.

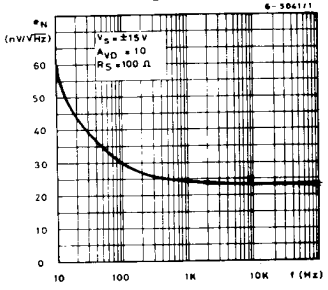


Fig. 11 - Total harmonic distortion vs. frequency.

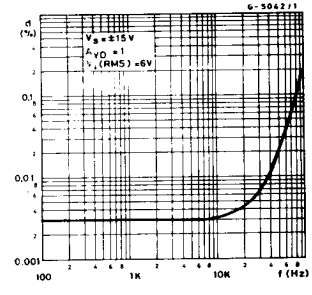
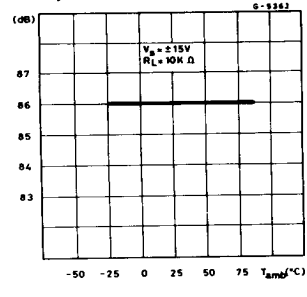
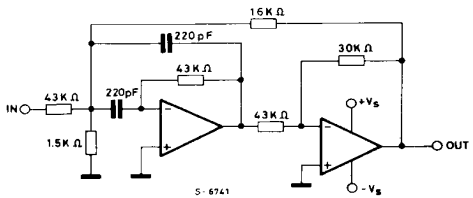


Fig. 12 - Common mode rejection vs. temperature



APPLICATION INFORMATION

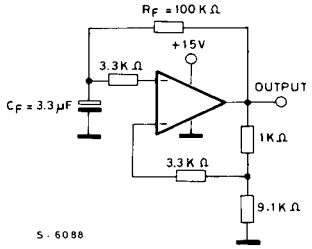
Fig. 13 - Second order high Q band pass filter (f_o = 100 KHz, Q = 30, gain = 4)



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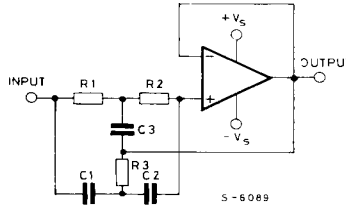
APPLICATION INFORMATION

Fig. 14 - 0.5 Hz square wave oscillator



$$f = \frac{1}{2\pi R_F C_F}$$

Fig. 15 - High Q Notch filter

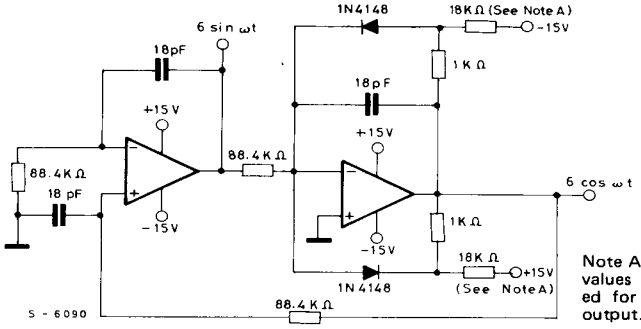


$$R1 = R2 = 2R3 = 1.5M\Omega$$

$$C1 = C2 = \frac{C3}{2} = 110\ pF$$

$$f_o = \frac{1}{2\pi R1\ C1} = 1\ KHz$$

Fig. 16 - 100 KHz quadrature oscillator



Note A: These resistor values may be adjusted for a symmetrical output.

Fig. 17 - 20 Hz to 200 Hz variable High-pass filter (G_v= 3 dB)

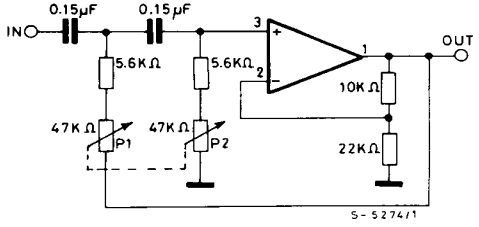
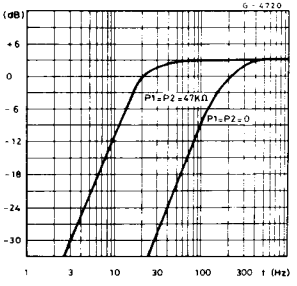


Fig. 18 - Frequency response of the high-pass filter of fig.17



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APPLICATION INFORMATION (continued)

Fig. 19 - Unity-gain absolute-value circuit

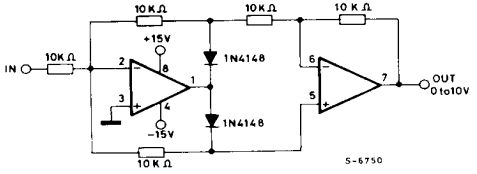


Fig. 20 - Single supply sample and hold

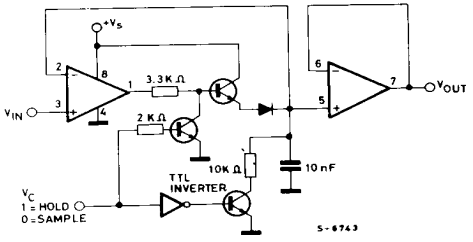
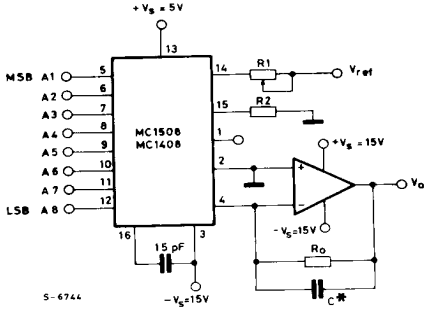


Fig. 21 - Output current to voltage transformation for a DA converter



(*) The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF).

Settling time to within 1/2 LSB (± 19.5 mV) is approximately 4.0 μs from the time all bits are switched.

Theoretical V_o :

$$V_o = \frac{V_{ref}}{R1}(R_o)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

Adjust V_{ref}, R1 or R_o so that V_o with all digital inputs at high level is equal to 9.961 volts.

$V_{ref} = 2.0\ V_{dc}$
$R1 = R2 \approx 1.0\ k\Omega$
$R_o = 5.0\ k\Omega$

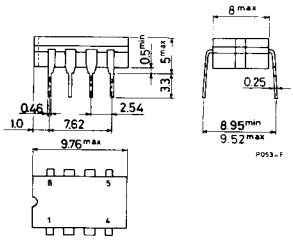
$$V_o = \frac{2\ V}{1\ k}(5\ k)\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right]$$

$$= 10V\left[\frac{255}{256}\right] = 9.961V$$

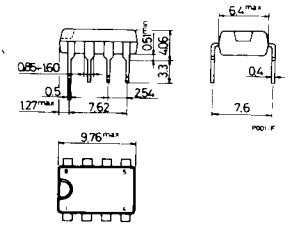
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MECHANICAL DATA (Dimensions in mm)

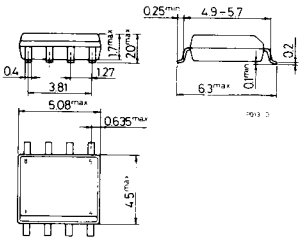
Minidip (Ceramic)



Minidip (Plastic)



SO-8 (Micropackage)



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