DATA SHEET

UV1316 MK4
VHF/UHF/Hyperband PAL TV tuner

Product specification

Approval by : 
Name / Date : Lim Kui Yong / 05.11.2004

PHILIPS

FEATURES



- Member of UV1300 MK4 family of small-sized full band tuners
- Systems CCIR: B/G, H, L, L', I and I'; OIRT: D/K
- Digitally-controlled (PLL) tuning via I^2C-bus
- Reduced power consumption
- Software controlled weak signal booster
- Off-air, S-cable and hyperband channels from 48.25 MHz to 863.25MHz inclusive
- World standardized mechanical dimensions and pinning. Horizontal mounting is optionally available
- Various connector types available

ORDERING INFORMATION

TYPE	DESCRIPTION	ORDER NUMBER
UV1316/A I-4	Asymmetrical IF, IEC	3139 147 20691
UV1316/S I-4	Symmetrical IF, IEC	3139 147 20891
UV1316/S I H-4	Symmetrical IF, IEC, horizontal mount	3139 147 22111
UV1316/A I H-4	Asymmetrical IF, IEC, horizontal mount	3139 147 22101
UV1316/A L-4	Asymmetrical IF, IEC long	3139 147 22301
UV1316/A P-4	Asymmetrical IF, phono	3139 147 22411
UV1316/A L-H-4	Asymmetrical IF, IEC long, horizontial mount	3139 147 22421
UV1316/S L-4	Symmetrical IF, IEC long	3139 147 24111

MARKING

The following items of information are printed on a sticker that is on the top cover of the tuner:

- Type number
- Code number
- Origin letter of factory
- Change code
- Year and week code

DESCRIPTION

The UV1316 MK4 tuner belongs to the UV1300 family of fourth generation WSP tuners, which are designed to meet a wide range of TV applications. It is a full band tuner suitable for CCIR systems B/G, H, L, L', I and I'. The low IF output impedance is designed for direct drive of a wide variety of SAW filters with sufficient suppression of triple transient.

The UV1316 MK4 is backwards compatible with its predecessors, the UV1316 MK1, MK2 and MK3. In addition, a 5 level Analog Digital Converter comes standard with the MK4.

This tuner complies with the requirements of radiation, signal handling capability and immunity conforming to:

- CISPR 13 (1990) incl. amendment 1 (1992) and amendment 2 (1993)
- European standards CENELEC EN55013, EN55020
- CISPR13 (4th Edition)

INTERMEDIATE FREQUENCIES

SIGNAL	FREQUENCY(1) (MHz)				
	SYSTEM B/G, H	SYSTEM L	SYSTEM L'(2)	SYSTEM I	SYSTEM I'
Picture carrier	38.90	38.90	33.40	39.50	38.90
Color	34.47	34.47	37.83	35.07	34.47
Sound 1	33.40	32.40	39.90	33.50	32.90
Sound 2	33.16	-	-	33.00	32.40

Notes

(1) The oscillator frequency is above the input signal frequency.

(2) Does not cover channel FA.

CHANNEL COVERAGE

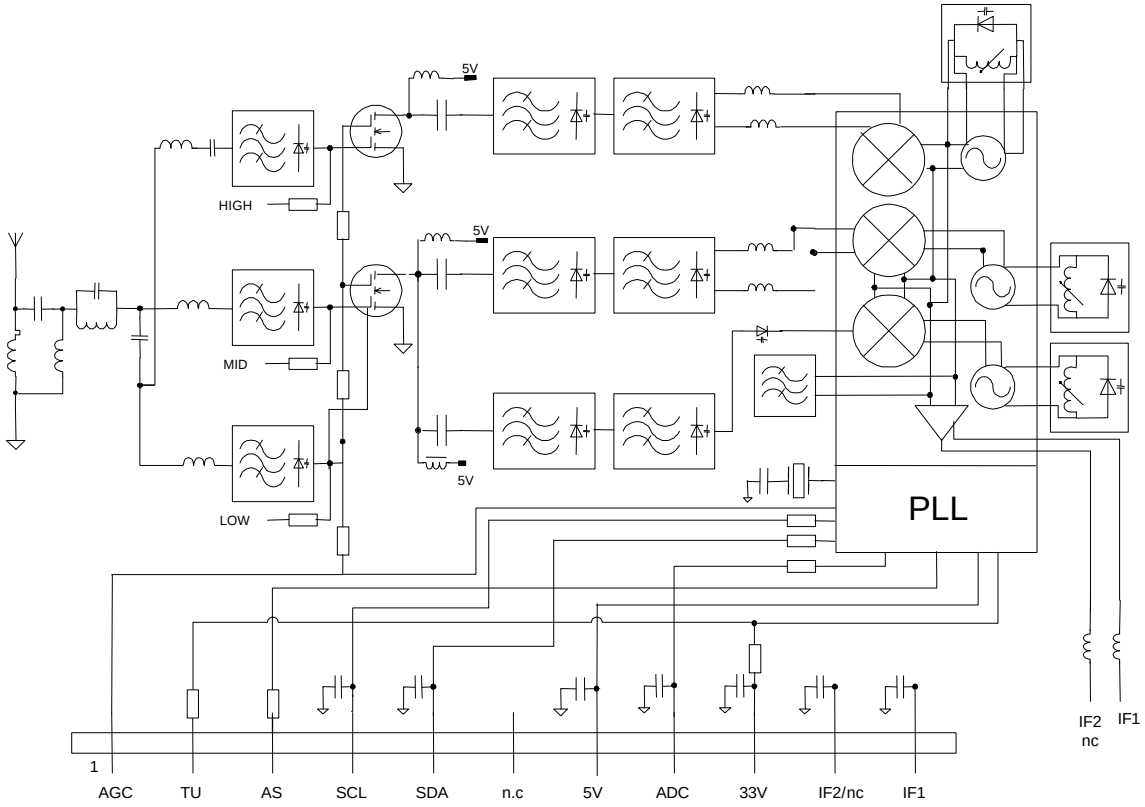
BAND	OFF-AIR CHANNELS		CABLE CHANNELS	
	CHANNELS	FREQUENCY RANGE (MHz)	CHANNELS	FREQUENCY RANGE (MHz)
Low band	E2 to C	48.25 to 82.25 (3)	S01 to S08	69.25 to 154.25
Mid band	E5 to E12	175.25 to 224.25	S09 to S38	161.25 to 439.25
High band	E21 to E69	471.25 to 855.25 (4)	S39 to S41	447.25 to 463.25

Notes

(3) Sufficient margin is available to tune down to 44.00MHz.

(4) Sufficient margin is available to tune up to 865.25MHz.

BLOCK DIAGRAM



PINNING

SYMBOL	PIN	DESCRIPTION
AGC	1	Automatic Gain Control Voltage
TU	2	Tuning voltage monitor (output)
AS	3	I ^{2}C-Bus Address Select
SCL	4	I ^{2}C-Bus Serial Clock
SDA	5	I ^{2}C-Bus Serial Data
n.c.	6	Not Connected
V_s	7	Supply Voltage +5V
ADC	8	ADC Input (5)
V_{ST}	9	Fixed tuning Supply Voltage +33V
I.F out 2 / d.n.c	10	Symmetrical I.F output 2 / Do not connect for asymmetrical
I.F out 1	11	Asymmetrical I.F Output / Symmetrical I.F output 1
GND	M1,M2,M3,M4	Mounting Tags (Ground)

NOTE
(5) Standard 5 level Analog to Digital Converter

LIMITING VALUES

Environmental conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Non-operational Conditions					
T_{AMB}	Ambient temperature		-25	+85	°C
RH	Relative humidity		-	95	%
g_B	Bump acceleration	25g	-	245	m/s^2
g_S	Shock acceleration	50g	-	490	m/s^2
	Vibration amplitude	10 to 55 Hz	-	0.35	mm
Operational conditions					
T_{AMB}	Ambient temperature		-10	+65	°C
RH	Relative humidity		-	95	%

Limiting values under operational conditions

The tuner can be guaranteed to function properly under the following conditions.

SYMBOL	PARAMETER	PIN	MIN	TYP.	MAX.	UNIT
V_S	Supply voltage	7	4.75	5.00	5.50	V
$V_{S(ripple)}$	Peak to peak ripple voltage susceptibility(6)		10	-	-	mV
I_s	Supply current		-	-	100	mA
V_{ST}	Tuning supply voltage	9	30	33	35	V
$V_{ST(ripple)}$	Peak to peak ripple voltage susceptibility		10	-	-	mV
I_{ST}	Tuning supply current		-	-	1.7	mA
V_{AGC}	AGC input voltage	1	-	4.0	4.5	V
ΔV_{AGC}	AGC input voltage range		0.5	-	4.0	V
I_{AGC}	AGC input current		-	-	20	µA
V_{AS}	Address select input voltage	3	-	-	5.5	V
V_{SCL}	Serial clock input voltage	4	-0.3	-	5.5	V
V_{SDA}	Serial data input voltage	5	-0.3	-	5.5	V
I_{SDA}	Serial data input current		-1	-	5	mA

NOTE

(6) Sinusoidal ripple voltage superimposed on the 5V-supply voltage in the frequency range of 15 kHz to 500 kHz. Criteria for TV interference is >57 dB.

ELECTRICAL DATA

Conditional data

Unless otherwise specified, all electrical values for Chapter “Electrical data” apply at the following conditions and the electrical performance is related to system B,G and H.
A proper function is guaranteed within the specified operational conditions but a certain deterioration of performance parameters may occur at the limits of operational conditions.

SYMBOL	PARAMETER	VALUE	UNIT
T_{AMB}	Ambient temperature	25 ± 5	^{o}C
RH	Relative humidity	60 ± 15	%
V_S	Supply voltage +5V	5 ± 0.125	V
V_{AGC}	AGC supply voltage	4 ± 0.1	V
V_{ST}	Tuning supply voltage	33 ± 0.5	V
t_{pr}	Pre-heating time (+5V at pin 7)	10	Minutes
$Z_{S(AE)}$	Aerial source impedance (unbalanced)	75	Ω

Aerial input characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
VSWR	Reflection coefficient referred to 75Ω impedance	Picture carrier at maximum gain	-	5	
V_{ant}	Antenna connection disturbance voltage	< 950 MHz	-	46	dBµV
		0.950 < f < 2.15 GHz	-	54	dBµV

GENERAL CHARACTERISTICS

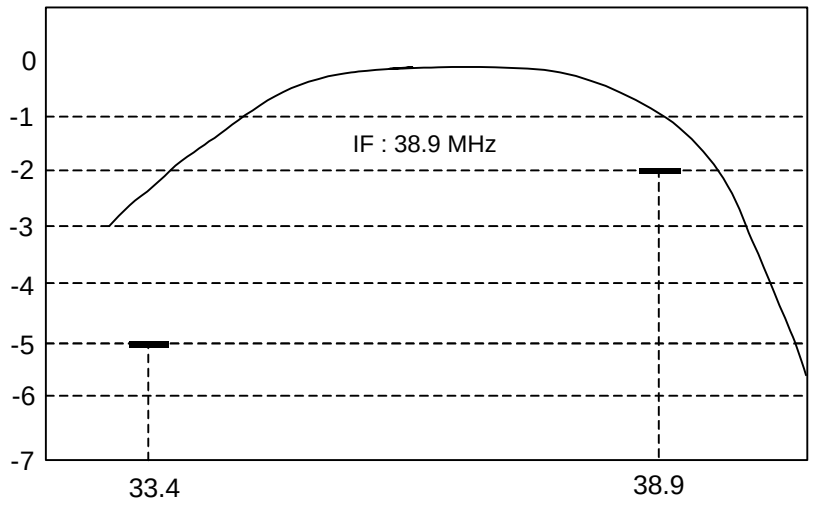
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_B	**Frequency range:**					
	Low band		48.25	-	154.25	MHz
	Mid band		161.25	-	439.25	MHz
	High band		447.25	-	855.25	MHz
Δf_B	**Margin:**					
	For low band end (negative)		-2/+3	-	-	MHz
	For mid/high band		±3	-	-	MHz
G_v	**Voltage gain:**					
	Low and Mid band		40	45	-	dB
	High band		40	45	-	dB
	Gain taper - (All off-air channels)		-	-	8	dB
	Noise:					
	Low band		-	5	9	dB
	Mid band		-	5	9	dB
	High band		-	5	9	dB
ΔV_{AGC}	**AGC input voltage range:**					
	Low Band		40	50	-	dB
	Mid Band		40	50	-	dB
	High band		35	45	-	dB
α_i	**Image rejection** (nominal gain to 10 dB gain reduction):					
	Low and mid band	< 300 MHz	66	75	-	dB
	Mid band	> 300 MHz	60	78	-	dB
	High band		50	55	-	dB
α_{IF}	**IF rejection (picture)**		60	80	-	dB
	½ IF Susceptibility		60	80	-	dBµV
$\alpha_{1/2RF}$	**½ RF Rejection**		60	-	-	dB
α_S	**Sound-chroma moire rejection:**					
	Off-air	Up to 40dB gain reduction	56	65	-	dB
	UHF	Up to 30dB gain reduction	56	75	-	dB
m_x	**Cross modulation:**					
	In-band					
	All bands (n±1)		66	-	-	dBµV
	Low band (n±2)		70	82	-	dBµV
	Mid band(n±2)		70	82	-	dBµV
	High band(n±2)		68	80	-	dBµV
	Out of band		-	100	-	dBµV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{OSC}	**Oscillator voltage:**					
	IF pin		-	70	85	dBµV
	All other pins		-	50	70	dBµV
	Overloading:					
	1dB gain compression		74	81	-	dBµV
	PLL lock-out		90	-	-	dBµV
	Tuning system interference:					
	Crystal harmonics interference rejection at IF output	Input level 50 dBµV	54	-	-	dB
	Divider interference rejection at IF output		57	-	-	dB
	Residual FM caused by IIC x-talk		-	-	5	kHz
V_{ESD}	Electrostatic discharge (ESD) on all pins	Note 1	2	-	-	kV
V_{SURGE}	- On Antenna		4	-	-	kV
	- On Ground Pin		TBF			
	Oscillator characteristics:					
	Oscillator tuning resolution	Note 2	31.25	-		kHz
	Lock-in time		-	-	100	msec

NOTE

1. All the pins of the tuner are protected against electrostatic discharge (ESD) up to 2 kV. The product is in accordance with EIA/JES022-A114-A
2. Resolution 31.25kHz, 50.00kHz or 62.5 kHz (see table “Ratio select bits”)

AMPLITUDE RESPONSE



The tilt of the response curve is defined as the difference from the top to the corresponding picture or sound carriers.

Fig. 2b Amplitude response curve (tilt)

VISIBILITY TEST (INPUT IMMUNITY AND IMMUNITY FROM RADIATED FIELDS)

The tuners meet the requirements of the European Standard "*EN55020*", when measured in an adequate television receiver[1]. The external AGC must be adjusted so that the picture carrier level (top sync) at the tuner output does not exceed 107 dBµV at an input signal level of 74 dBµV or greater.

Refer to section **IF LOAD** on page 14 for more details.

RADIATION

The tuners meet the requirements of the European Standard "*EN55013*" and "*CISPR13*" (1990), when measured in an adequate television receiver[1].

Note 1 : Or measured in our reference application board.

APPLICATION INFORMATION

A detailed description of the I²C-bus specification, with applications, is given in brochure "The I²C-bus and how to use it". This brochure may be ordered using the code number 9398 393 40011.

Table 1 I²C-bus data format, *'WRITE'* mode

NAME	BYTE	7				BITS			0	ACK
		MSB							LSB	
Address Byte	ADB	1	1	0	0	0	MA1	MA0	R/$\overline{W}$=0	A
Prog. Div. Byte 1	DB1	0	N14	N13	N12	N11	N10	N9	N8	A
Prog. Div. Byte 2	DB2	N7	N6	N5	N4	N3	N2	N1	N0	A
Control Byte	CB	1	CP	T2	T1	T0	RSA	RSB	WSB	A
Band-switch byte	BB	X	X	X	P4	P3	P2	P1	P0	A

Table 2 Description of symbols used in Table 1

BIT	DESCRIPTION
MA1 and MA0	Programmable address bits (see Table 3)
R/W	Logic 0 for write mode
N14 to N0	Programmable divider bits; $N=N14x2^{14}+ N13x2^{13}+\ldots+ N1x2^{1}+N0$
CP	Charge pump current control bit: Logic 0 : Charge pump current is 20µA Logic 1 : Charge pump current is 100µA
T2,T1 and T0	Test bits (see table 4)
RSA and RSB	Reference divider ratio select bits (see Table 5)
WSB	Weak Signal Booster control bit Logic 0 : normal mode – no gain increase : IF filter is used Logic 1 : Weak Signal Booster activated : IF filter is by-passed
P0,P1,P2,P3,P4	Ports control bits : Logic 0 : Corresponding Port is "OFF". High impedance state (default) Logic 1 : Corresponding Port is "ON".

I^2C-bus address selection

The module address contains programmable address bits (MA1 and MA0) which offer the possibility of having several synthesizers (up to 4) in one system by applying a specific voltage on the AS input. The relationship between MA1 and MA0 and the input voltage applied to the AS input is given in Table 3.

Table 3 ADDRESS SELECTION

MA1	MA0	ADDRESS	VOLTAGE APPLIED ON AS INPUT
0	0	C0	0V to $0.1xV_{CC}$
0	1	C2	Open or $0.2xV_{CC}$ to $0.3xV_{CC}$
1	0	C4	$0.4xV_{CC}$ to $0.6xV_{CC}$
1	1	C6	$0.9xV_{CC}$ to $1.0xV_{CC}$

Table 4 TEST MODES

T2	T1	T0	TEST MODES
0	0	0	Normal mode
0	0	1	Normal mode (1)
0	1	0	Charge-pump is 'OFF' (3)
0	1	1	Byte BB ignored
1	1	0	Charge-pump is sinking current
1	1	1	Charge-pump is sourcing current
1	0	0	½ f_{REF} is available on port P3 (2)
1	0	1	½ f_{DIV} is available on port P3 (2)

Notes

1. This is the default mode at ***Power-On Reset***
2. The P3 port cannot be used when these test modes are active
3. ½ f_{REF} is available on port P3

Table 5 REFERENCE DIVIDER RATIO SELECT BITS

RSA	RSB	REFERENCE DIVIDER RATIO	STEP SIZE (kHz)
X	0	80	50 (1)
0	1	128	31.25 (1)
1	1	64	62.5 (1)

Notes

1. Crystal frequency or signal at XTIN of 4 MHz.

CONTROL BYTE 2 :

Band switching	0	0	0	P4	P3	P2	P1	P0
Low Band	0	0	0	0	0	0	0	1
Mid Band	0	0	0	0	0	0	1	0
High Band	0	0	0	0	0	1	0	0

Ports 0 to 3 control the bandswitching.

TELEGRAM EXAMPLES (WRITE MODE):

Start – ADB – ACK – DB1 – ACK – DB2 – ACK – Stop
Start – ADB – ACK – CB – ACK – BB – ACK – Stop
Start – ADB – ACK – CB – ACK – Stop
Start – ADB – ACK – DB1 – ACK – DB2 – ACK – CB – ACK - BB – ACK – Stop
Start – ADB – ACK – CB – ACK – BB – ACK - DB1 – ACK – DB2 – ACK – Stop
Start – ADB – ACK – DB1 – ACK – DB2 – ACK – CB – ACK – Stop

Note:

Start = start condition
ADB = address byte
ACK = acknowledge
DB1 = divider byte 1
DB2 = divider byte 2
CB = control byte
BB = band-switch byte
Stop = stop condition

For channel selection involving band switching, in order to ensure smooth tuning to the desired channel without causing unnecessary charge pump action, it is recommended to consider the difference between wanted channel frequency (fw) and the current channel frequency (fc):

- If fw > fc, use telegram as :

Start – ADB – ACK - DB1 – ACK – DB2 – ACK - CB – ACK - BB – ACK – Stop

- If fw < fc, use telegram as :

Start – ADB – ACK - CB – ACK – BB – ACK - DB1 – ACK - DB2 – ACK – Stop

Unnecessary charge pump action will result in very low tuning voltage ($V_T \approx 0V$) which may drive the oscillator to extreme conditions. Refer to Table 2 for recommendations on how to set the charge pump (CP) .

READ MODE; R/W = 1 (see Table 7)

Data can be read from the device by setting R/W bit to 1. After the slave address has been recognised, the device generates an ACKnowledge pulse and the first DATA byte (status byte) is transferred on the SDA line (MSB first). DATA is valid on the SDA line during a HIGH-level of the SCL clock signal. A second DATA byte can be read from the device if the microcontroller generates an ACKnowledge on the SDA line (master ACKnowledge). End of transmission will occur if no master ACKnowledge occurs. The device will then release the DATA line to allow the microcontroller to generate a STOP condition.

The POR flag is set to 1 at power-on. The flag is reset when an end-of-data is detected by the device (end of a READ sequence). Control of the loop is made possible with the in-LOCK flag FL which indicates when the loop is locked (FL=1).

The internal AGC status can be known from bit AGC (AGC=1), which indicates when the selected take-over point is reached.

A built-in ADC is available on the P6/ADC pin. This converter can be used to apply AFC information to the microcontroller from the IF section of the television. The relationship between the bits A2,A1 and A0 is given in Table 8.

Table 6 *'READ'* data format

NAME	BYTE	BITS							
		MSB (1)							LSB
Address Byte	ADB	1	1	0	0	0	MA1	MA0	R/W=1
Status Byte	SB	POR	FL	1	1	1	A2	A1	A0

Note:
1. MSB is transmitted first.

Table 7 Description of the bits used in Table 6

BIT	DESCRIPTION
MA1 and MA0	Programmable address bits (see Table 3)
R/W	Logic 1 for read mode
POR	Power-on reset flag : Logic 0 : after end of the first read sequence Logic 1 : at power-on
FL	In-lock flag : Logic 0 : loop is not locked Logic 1 : loop is locked
A2,A1 and A0	Digital outputs of the 5-level ADC (see Table 8)

Table 8 ADC digital outputs (1)

A2	A1	A0	VOLTAGE APPLIED ON ADC INPUT
1	0	0	$0.6xV_{CC}$ to 5.5V
0	1	1	$0.45xV_{CC}$ to $0.6xV_{CC}$
0	1	0	$0.30xV_{CC}$ to $0.45xV_{CC}$
0	0	1	$0.15xV_{CC}$ to $0.30xV_{CC}$
0	0	0	0 to $0.15xV_{CC}$

Note:
1. Accuracy is $\pm$ 0.03 x V_{CC}
2. No erratic codes in the transition

TELEGRAM EXAMPLES (*READ* MODE):

Start – AB (R/W=1) – XX[(1)] – X[(2)] – Stop
Start – AB (R/W=1) – XX[(1)] – ACK – XX[(1)] – X[(2)] – Stop

Notes
(1) XX = Read status byte
(2) X = No ACKnowledge from the master means end of sequence

POWER–ON RESET

The power-on detection threshold voltage VPOR is set to tbf V at room temperature. Below this threshold the device is reset to the power-on state.

At power-on state the following actions take place :

- The charge pump current is set to 100 μA
- The test bits T2, T1 and T0 are set to logic ‘001’. The charge pump can be either sinking or sourcing.
- The Weak Signal Booster is disabled
- All ports are OFF and the HIGH band is selected by default

Table 9 Default setting of the bits at *POWER-ON RESET*

NAME	BYTE	BITS							
		MSB							LSB
Address Byte	ADB	1	1	0	0	0	MA1	MA0	x
Divider Byte 1	DB1	0	x	x	x	x	x	x	X
Divider Byte 2	DB2	x	x	x	x	x	x	x	x
Control Byte	CB	1	1	1	1	0	x	x	0
Band Switch Byte	BB	X	X	X	0	0	0	0	0

TUNING SUPPLY VOLTAGE

Pin 9 must be set to a typical tuning voltage of 33V (maximum 35V and minimum 30V). Alternatively, a constant current of 1 to 1.5 mA can also be applied. Figure 3 shows an alternative supply from a 140V source. The Zener diode prevents the tuning voltage at pin 9 from exceeding 33V.

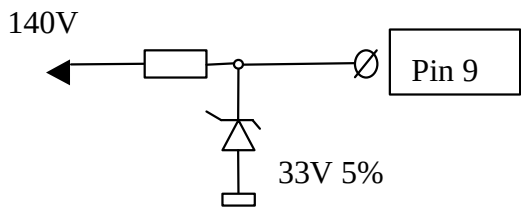


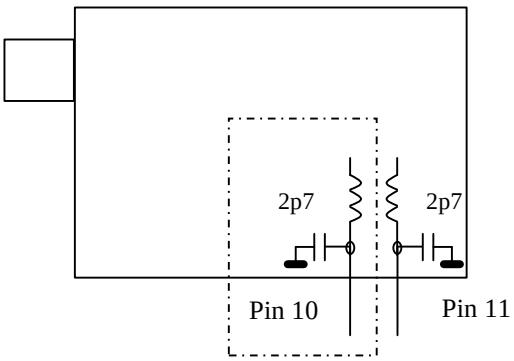
Fig. 3 33V tuning supply

I.F BANDWIDTH (3 dB)

The typical bandwidth is 12 MHz.

I.F OUTPUT IMPEDANCE
(measured at 36.15 MHz)

Asymmetrical : 37 + j54Ω
Symmetrical : 87.6 + j21Ω



* Dashed box for symmetrical only

I ^{2}C-BUS LOAD

The UV1316E MK3 has a series resistor of 370 Ω and 370 Ω respectively in each of the SCL and SDA lines and a shunt capacitance of 18pF to ground at the pins. A capacitive load of typically 56pF is allowed at these pins for standard 100kHz IIC bus mode. See Fig 4 below.

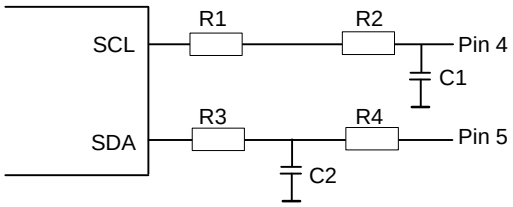


Fig 4. Internal I^{2}C bus loading

I.F LOAD

The maximum permissible resistive load is 280Ω, the maximum capacitive load is 40pF.

To guarantee optimum signal handling performance, the reactive load of the I.F circuitry (interconnections, saw filter) has to be tuned to tuner I.F center frequency according to the following formula:

$$L_{tune} = \{(2*\pi*f)^2 * (C_{int} + C_{stray} + C_{SAW})\}^{-1}$$

Where C_{int} = internal capacitance of the tuner
= 2.7pF for asymmetrical
= 1.35pF for symmetrical
C_{stray} = stray capacitance attributed to layout in the chassis
C_{SAW} = intrinsic capacitance of the SAW filter used/selected
f =desired I.F frequency, usually centered between picture and sound.

The IF output is to be maintained at 107 dBµV maximum. In case this limit is exceeded, the tuner gain should be reduced accordingly.

AUTOMATIC GAIN CONTROL (AGC)

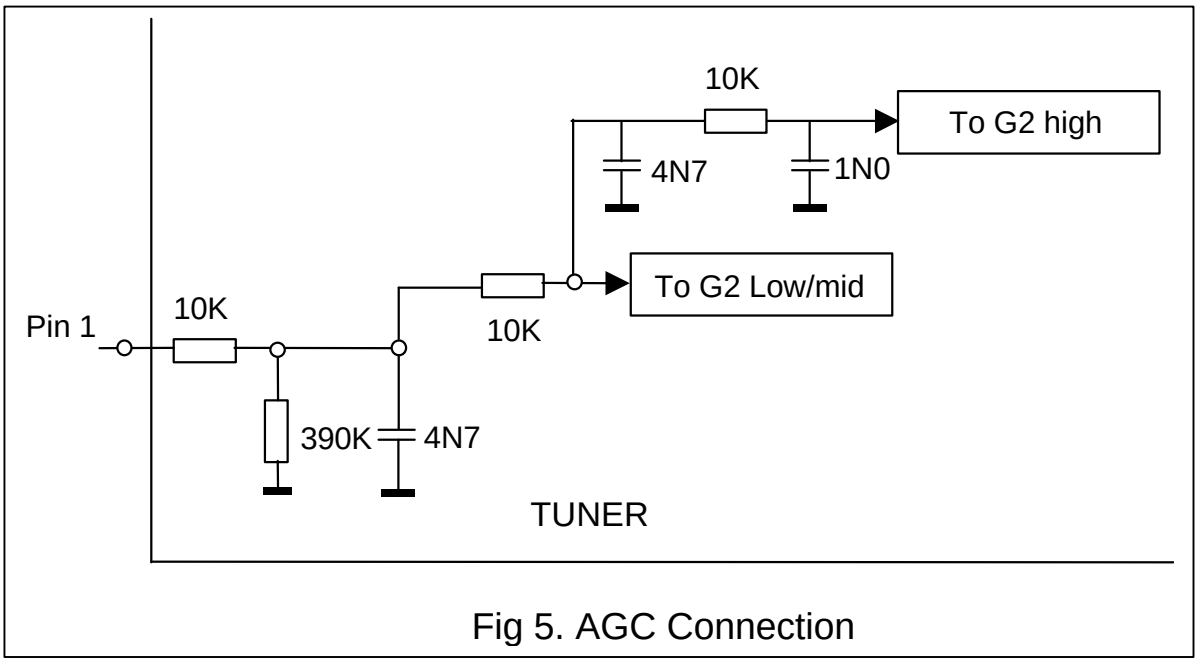
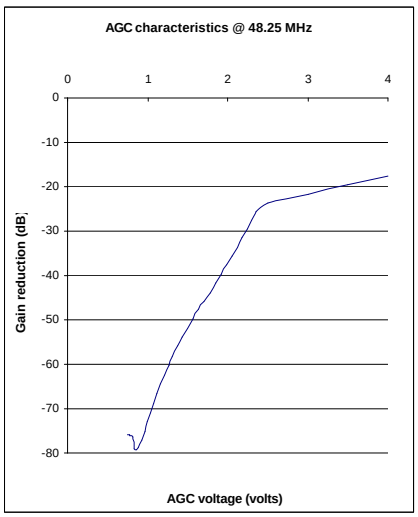
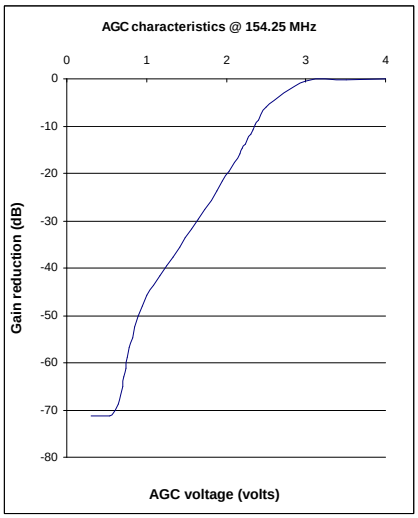


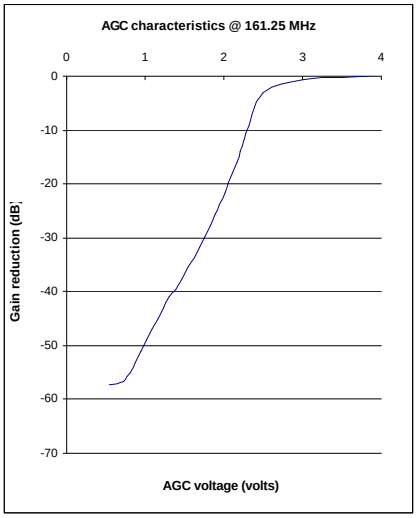
Fig 5. AGC Connection

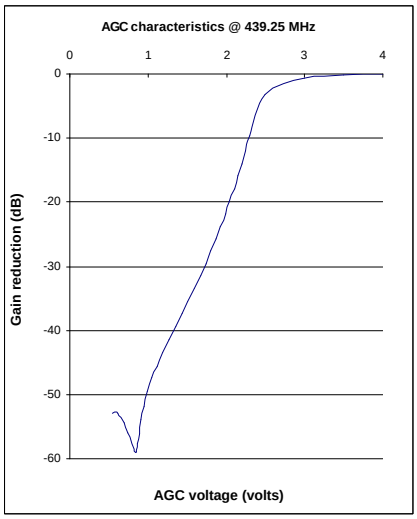
AGC Characteristics

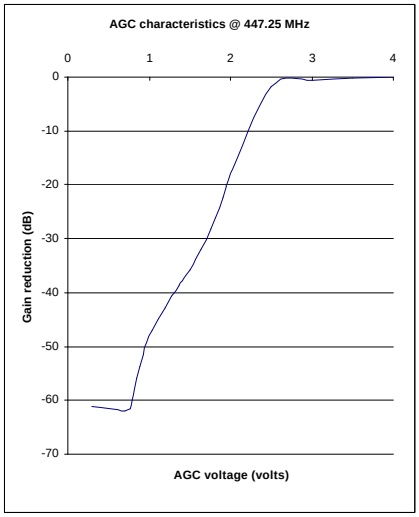
TYPICAL AGC CURVES

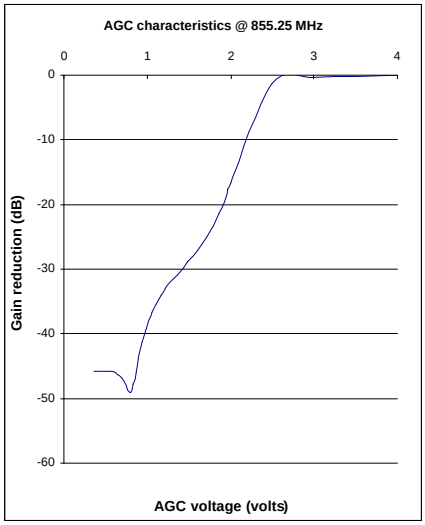












MECHANICAL DATA

See product drawing 3139 149 0157

AERIAL CONNECTIONS

Standard IEC socket female 75Ω.

SOLDERABILITY

The solderability of pins and mounting tags when tested initially and after 16 hour steam ageing in accordance with "*IEC 60068-2-20*", test Ta, method 1 (solder bath 235°C for 2s), results in a wetted area of 95%. No de-wetting will occur when soldered at 260°C for 5s.

RESISTANCE TO SOLDERING HEAT

The product will not be damaged when tested in accordance with "*IEC 60068-2-20*", test Tb, ,method 1A (solder bath 260°C for 10±1 s).

MASS

Approximately 34g (IEC)

ROBUSTNESS OF PINS

The pins will not be damaged when tested in accordance with "*IEC 60068-2-21*":

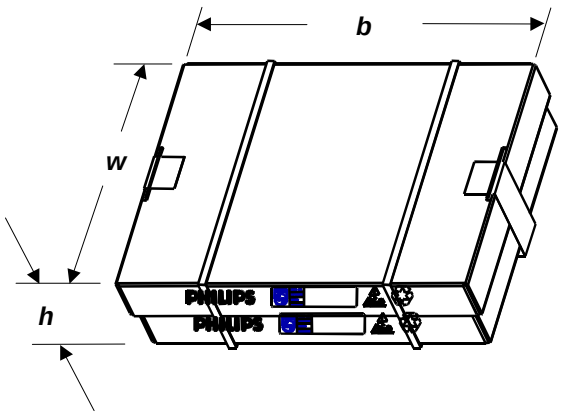
- Test Ua1, tensile of 10N in axial direction
- Test Ua2, thrust of 4N in axial direction

PUNCHING PATTERN OF CHASSIS PCB

For optimum mounting of the tuner to a PCB the following punching pattern is recommended (see 3139 149 0157).

The tuner must be mounted without clearance between the tuner supporting surface and the printed circuit board (PCB). When mounted in this way, the tuner must be soldered to the PCB. This can be achieved by pressing the unit vertically onto the PCB during soldering.

Example of Carton Box:

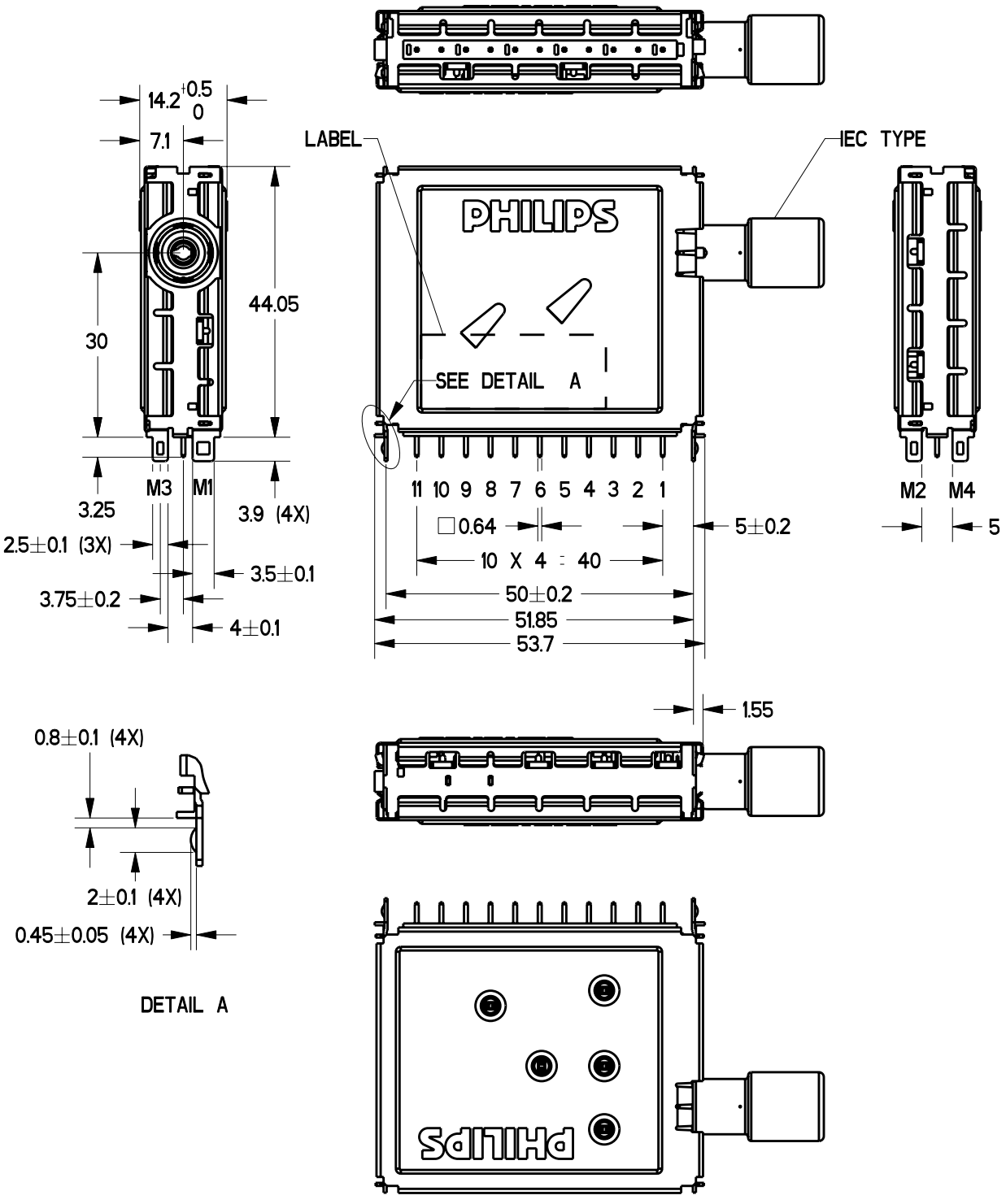


PACKAGING INFO

The products are packed in the carton box and transferred to customers by Pallet Transport.

Type		Vertical			Horizontal		
		Dimension b x w x h (cm)	No of sets	Gross wt (kg)	Dimension b x w x h (cm)	No of sets	Gross wt (kg)
IEC-I	Carton	46 x 34 x 7.5	98	3.9	46 x 34 x 9.4	60	3.04
	Pallet	120 x 105 x 105	7742	329.7	120 x 105 x 105	3900	219.6
IEC-L	Carton	46 x 34 x 8.2	98	3.91			
	Pallet	120 x 105 x 105	7056	303.6			

Carton Boxes are made of Corrugated Fibreboard which are free of environmentally banned substances.



VERTICAL MOUNTING

Note:
- General tolerance ±0.5 mm unless otherwise stated.
- All dimensions are in millimeter.
- Drawing not to scale.

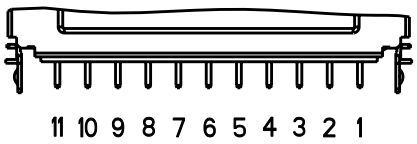
CLASS NO. 3UM900	PRODUCT DRAWING UV1300 MK4 MECHANICS	3139 149 0157	1 2004-05-04 1 2003-05-05 1 2003-08-12 1 2003-10-08 1 2004-03-23
2002-10-01			
NAME JOHNNY LU	SUPERS .	5 / 10 / 110 - 1	A4
SV / CHECK	DATE 2002-10-01	© KONINKLIJKE PHILIPS ELECTRONICS N.V.	

ALL RIGHTS ARE RESERVED. REPRODUCTION IN WHOLE OR IN PART IS PROHIBITED WITHOUT THE WRITTEN CONSENT OF THE COPYRIGHT OWNER.

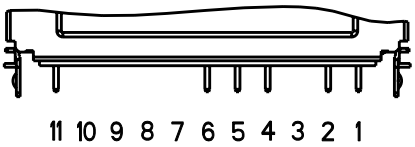
PHILIPS

ALL RIGHTS ARE RESERVED. REPRODUCTION IN WHOLE OR IN PART IS PROHIBITED WITHOUT THE WRITTEN CONSENT OF THE COPYRIGHT OWNER.

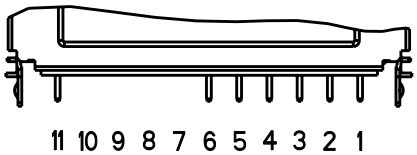
VARIOUS PINNING CONFIGURATION FOR VERTICAL MOUNTING



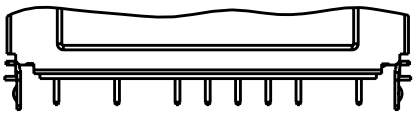
UV1316/16E MK4
UV1338 MK4
UV1336B MK4
UV1336BE MK4
UV1356E MK4



UV13X5C MK3 2 BIT BAND SWITCH
eg. UV13X5C/A I B-3

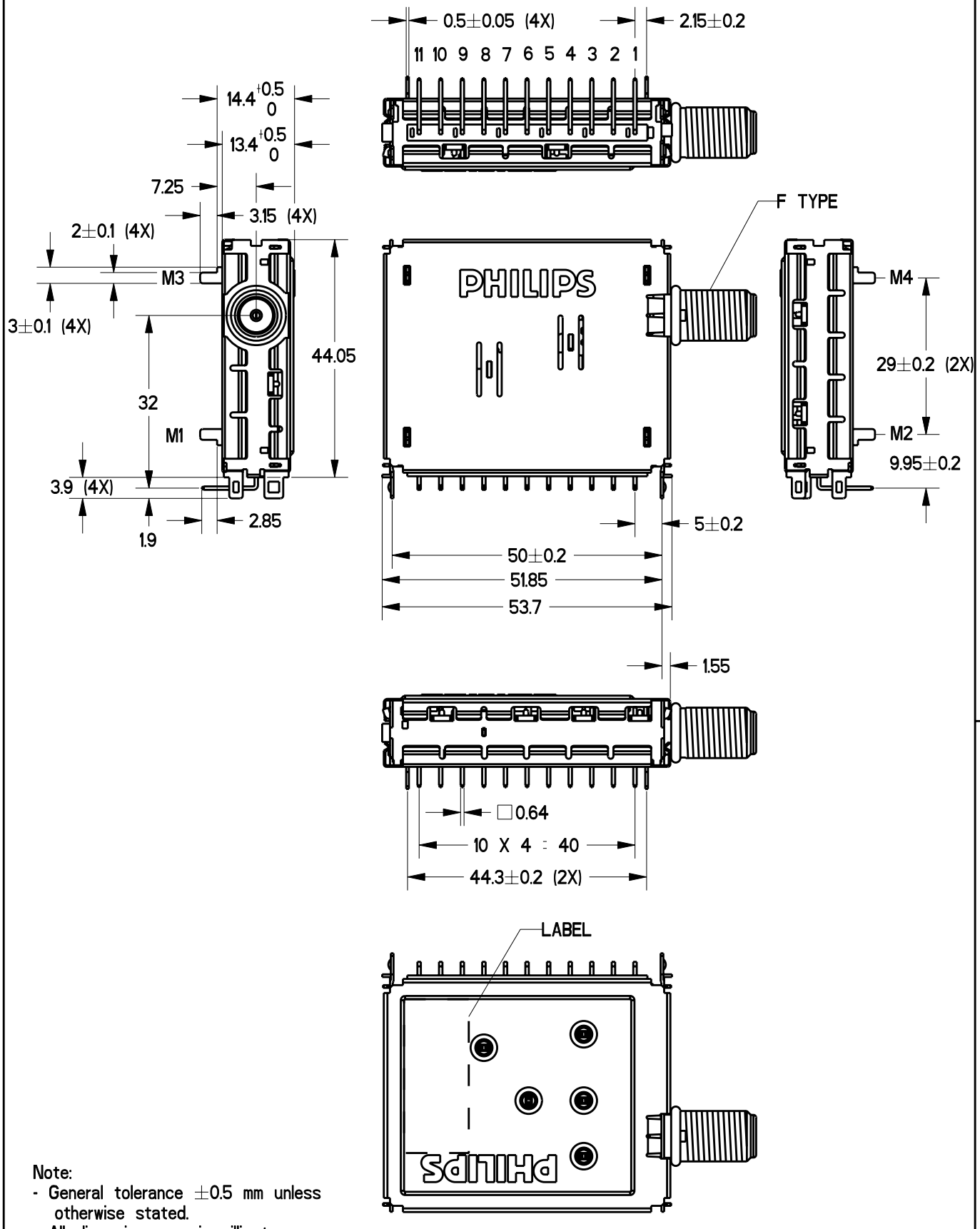


UV13X5C MK3 3 BIT BAND SWITCH



UV1356E/A L-4

CLASS NO. 3UM900	PRODUCT DRAWING UV1300 MK4 MECHANICS		3139 149 0157		1	2004-05-04	
.					1	2003-05-05	
.					1	2003-08-12	
2002-10-01					1	2003-10-08	
					1	2004-03-23	
NAME JOHNNY LU	SUPERS .	5	10	110 - 2		A4	
SV / CHECK	DATE 2002-10-01	© KONINKLIJKE PHILIPS ELECTRONICS N.V.					



Note:
- General tolerance ±0.5 mm unless otherwise stated.
- All dimensions are in millimeter.
- Drawing not to scale.

HORIZONTAL MOUNTING

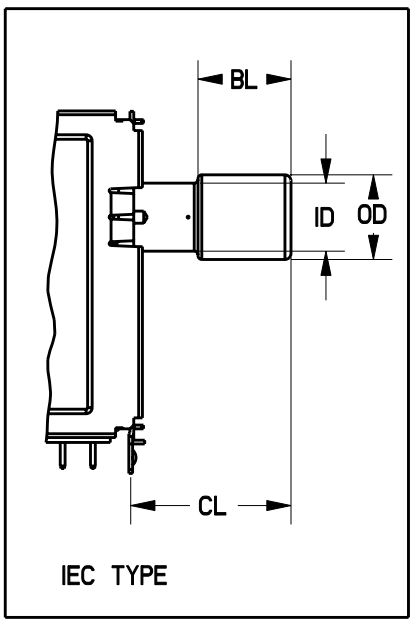
ALL RIGHTS ARE RESERVED. REPRODUCTION IN WHOLE OR IN PART IS PROHIBITED WITHOUT THE WRITTEN CONSENT OF THE COPYRIGHT OWNER.

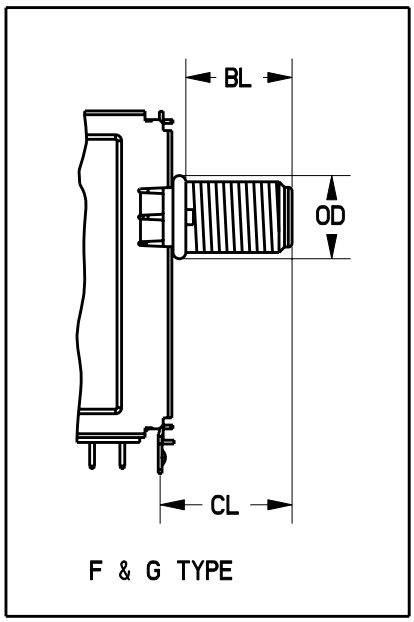
CLASS NO. 3UM900	PRODUCT DRAWING UV1300 MK4 MECHANICS	3139 149 0157	1 2004-05-04 1 2003-05-05 1 2003-08-12 1 2003-10-08 1 2004-03-23
2002-10-01			
NAME JOHNNY LU	SUPERS .	5 / 10 / 110 - 3	A4
SV / CHECK	DATE 2002-10-01	© KONINKLIJKE PHILIPS ELECTRONICS N.V.	

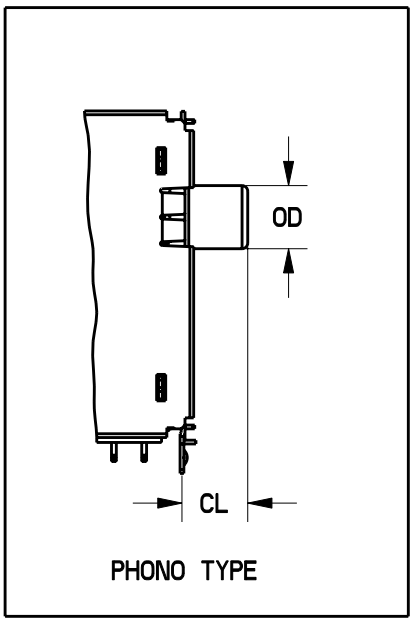
PHILIPS

ALL RIGHTS ARE RESERVED. REPRODUCTION IN WHOLE OR IN PART IS PROHIBITED WITHOUT THE WRITTEN CONSENT OF THE COPYRIGHT OWNER.

AERIAL CONNECTOR TYPE

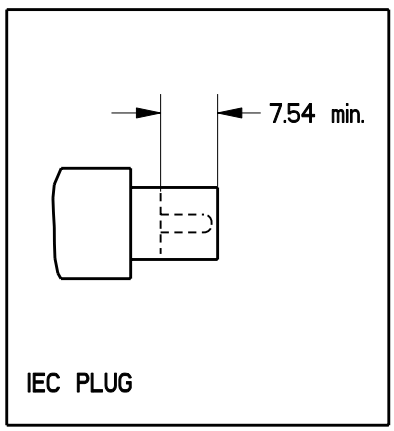


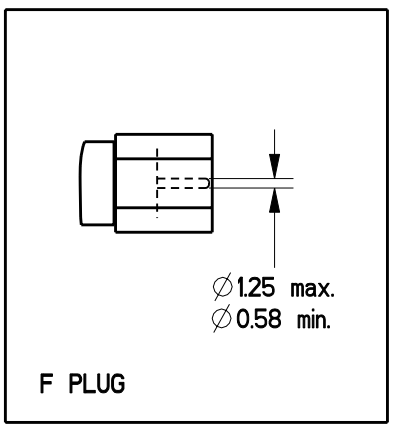


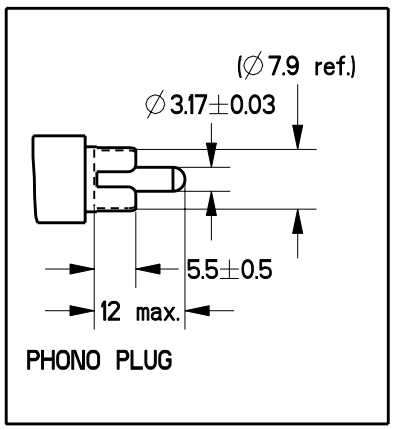


CONNECTOR TYPE	CONNECTOR LENGTH, CL	BODY LENGTH, BL	OVERALL DIAMETER, OD	INNER DIAMETER, ID
IEC-I	14.8±0.5	12.3±0.3	11.0±0.1	8.0±0.2
IEC-L	21.2±0.5	12.3±0.3	11.2±0.1	9.0±0.3
F-F	17.5±0.5	14.1±0.5	11.0±0.2	--
F-G	22.2±0.5	16.5±0.3	12.15±0.15	-
PHONO-P	8.7±0.5	--	8.35+0/-0.1	--

MALE CONNECTOR REQUIREMENT







For dimension which is not reflected in drawing, refer to IEC 60169-2 (for IEC plug) and IEC 60169-24 (for F plug).

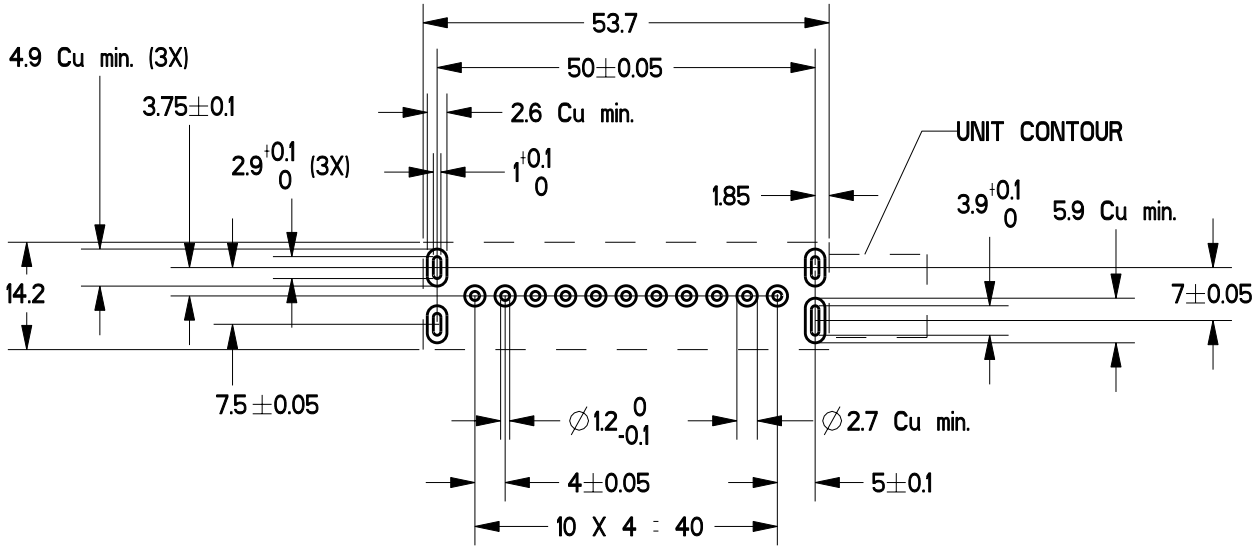
CLASS NO. 3UM900	PRODUCT DRAWING UV1300 MK4 MECHANICS	3139 149 0157	1 2004-05-04 1 2003-05-05 1 2003-08-12 1 2003-10-08 1 2004-03-23
2002-10-01			
NAME JOHNNY LU	SUPERS .	5 / 10 / 110 - 4	A4
SV / CHECK	DATE 2002-10-01	© KONINKLIJKE PHILIPS ELECTRONICS N.V.	

PHILIPS

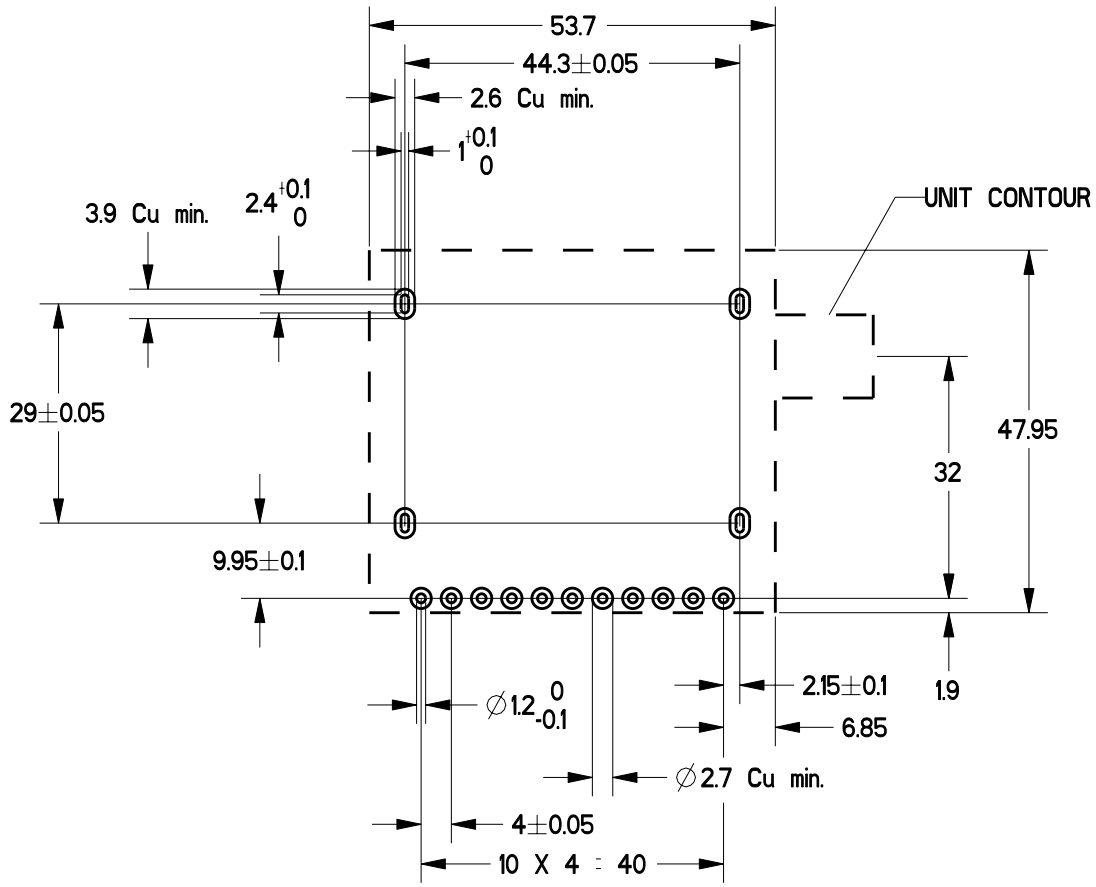
ALL RIGHTS ARE RESERVED. REPRODUCTION IN WHOLE OR IN PART IS PROHIBITED WITHOUT THE WRITTEN CONSENT OF THE COPYRIGHT OWNER.

PUNCHING PATTERN OF CHASSIS PCB

PUNCHING PATTERN SEEN FROM SOLDER SIDE



VERTICAL MOUNTING



HORIZONTAL MOUNTING

CLASS NO. 3UM900	PRODUCT DRAWING UV1300 MK4 MECHANICS	3139 149 0157	1	2004-05-04			
.			1	2003-05-05			
.			1	2003-08-12			
2002-10-01			1	2003-10-08			
			1	2004-03-23			
NAME JOHNNY LU	SUPERS .	5	10	110 - 5		A4	
SV	CHECK	DATE 2002-10-01	© KONINKLIJKE PHILIPS ELECTRONICS N.V.				

Document revision history

Rev #	Date	Approved by	Remarks
	03-01-15		draft create by Toh Yeow Teng
	03-01-22		draft - changes in pg 6
a	03-03-03		draft - changes in pg 2, 6, 7, 9 and last page
a	03-03-24		draft - changes in pg 2, 6, 10 to 15
a	03-04-07		draft - changes in pg 3, 6, 7, 9
a	03-04-22	Toh Yeow Teng	Trigger by Toh YT changes in pg 2, 6, 15, 16, 17 - 20
b	03-05-09	Toh Yeow Teng	Trigger by Toh YT Preliminary to Product, Updating pg 2, 8, 9, 15, 16
c	03-06-09	Toh Yeow Teng	Trigger by Toh YT Updating pg 6 only
d	03-09-10	Toh Yeow Teng	Trigger by Johnny Lu Updating Mechanical drawings
e	03-10-10	Ng Bee Theng	Trigger by Johnny Lu Updating Mechanical drawings
f	04-01-12	Ng Bee Theng	Trigger by Belle/Heng SH pg 2 - updating ordering information, pg 19 to 23 - mechanical drawings pg 26 – RF Solutions Sales Offices.
g	04-02-04	Alan Yeo	Trigger by Heng SH pg 19 – updating packing info
h	04-02-12	Toh Yeow Teng	Trigger by Heng SH/Daniel Lee pg 2 – ordering information (add 2 new type UV1316/A P-4 and UV1316/A L H-4) pg 20 to 24 – updating mechanical drawings
i	04-02-18	Toh Yeow Teng	Trigger by Daniel Lee; pg 3 – Intermediate frequencies (SYSTEM L' refer to note 2)
j	04-02-23	Toh Yeow Teng	Trigger by Daniel Lee, pg 2 – ordering information description change for UV1316/A P-4 pg 3 – updating note 2 should be Does not cover channel FA
k	04-05-20	Toh Yeow Teng	Trigger by Heng SH; Updating Mechanical drawings
L	04-11-05	Lim Kui Yong	Trigger by Belle Ng; Pg 2 : add new type no. UV1316/S L-4

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specification.
Application Information	
Where application information is given, it is advisory and does not form part of the specification	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I^{2}C COMPONENTS

Purchase of Philips I^{2}C components conveys a license under the Philips I^{2}C patent to use the components in the I^{2}C systems to the I^{2}C specification defined by Philips.
This specification can be ordered using the code 9398 393 40011.

RF Solutions Sales Offices

Refer to : Internet: www.rfsolutions.philips.com

© Philips Electronics N.V. 2004.
All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.