September 1995
Edition 6.0a

FUJITSU

DATA SHEET

MB1501/MB1501H/MB1501L

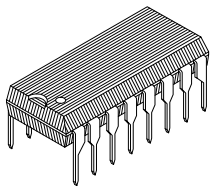
SERIAL INPUT PLL FREQUENCY SYNTHESIZER

SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH 1.1GHz PRESCALER

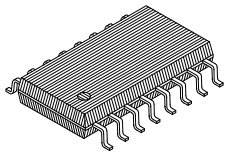
The Fujitsu MB1501/MB1501H/MB1501L, utilizing BI-CMOS technology, is a single chip serial input PLL frequency synthesizer with pulse-swallow function.

The MB1501 series contain a 1.1GHz two modulus prescaler that can select either 64/65 or 128/129 divide ratio; control signal generator; 16-bit shift register; 15-bit latch; programmable reference divider (binary 14-bit programmable reference counter); 1-bit switch counter; phase comparator with phase inverse function; charge pump; crystal oscillator; 19-bit shift register; 18-bit latch; programmable divider (binary 7-bit swallow counter and binary 11-bit programmable counter).

The MB1501 operates on a low supply voltage (3V typ) and consumes low power (45mW at 1.1GHz).



PLASTIC PACKAGE
DIP-16P-M04



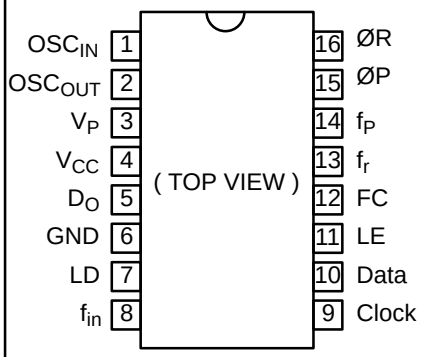
PLASTIC PACKAGE
FPT-16P-M06

MB1501 Product Line

	V_P Voltage	V_{OOP} Voltage	Lock up time	D_O Output Width	High-level Output Current	Low-level Output Current
MB1501	8V max	8.5V max	Middle speed	Middle	Middle	Middle
MB1501H	10V max	10.0V max	High speed	Low	High	Low
MB1501L	8V max	8.5V max	Low speed	High	Low	High

- High operating frequency: $f_{IN\ MAX}$=1.1GHz ($P_{IN\ MIN}$=0.20V_{P-P})
- On-chip prescaler
- Low power supply voltage: 2.7V to 5.5V (3.0V typ)
- Low power supply consumption: 45mW (3.0V, 1.1GHz operation)
- Serial input 18-bit programmable divider consisting of:
  - Binary 7-bit swallow counter (Divide ratio: 0 to 127)
  - Binary 11-bit programmable counter (Divide ratio: 16 to 2047)
- Serial input 15-bit programmable reference divider consisting of:
  - Binary 14-bit programmable reference counter (Divide ratio: 8 to 16383)
  - 1-bit switch counter (SW) Sets divide ratio of prescaler
- 2types of phase detector output
  - On-chip charge pump (Bipolar type)
  - Output for external charge pump
- Wide operating temperature: T_A=–40°C to +85°C

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

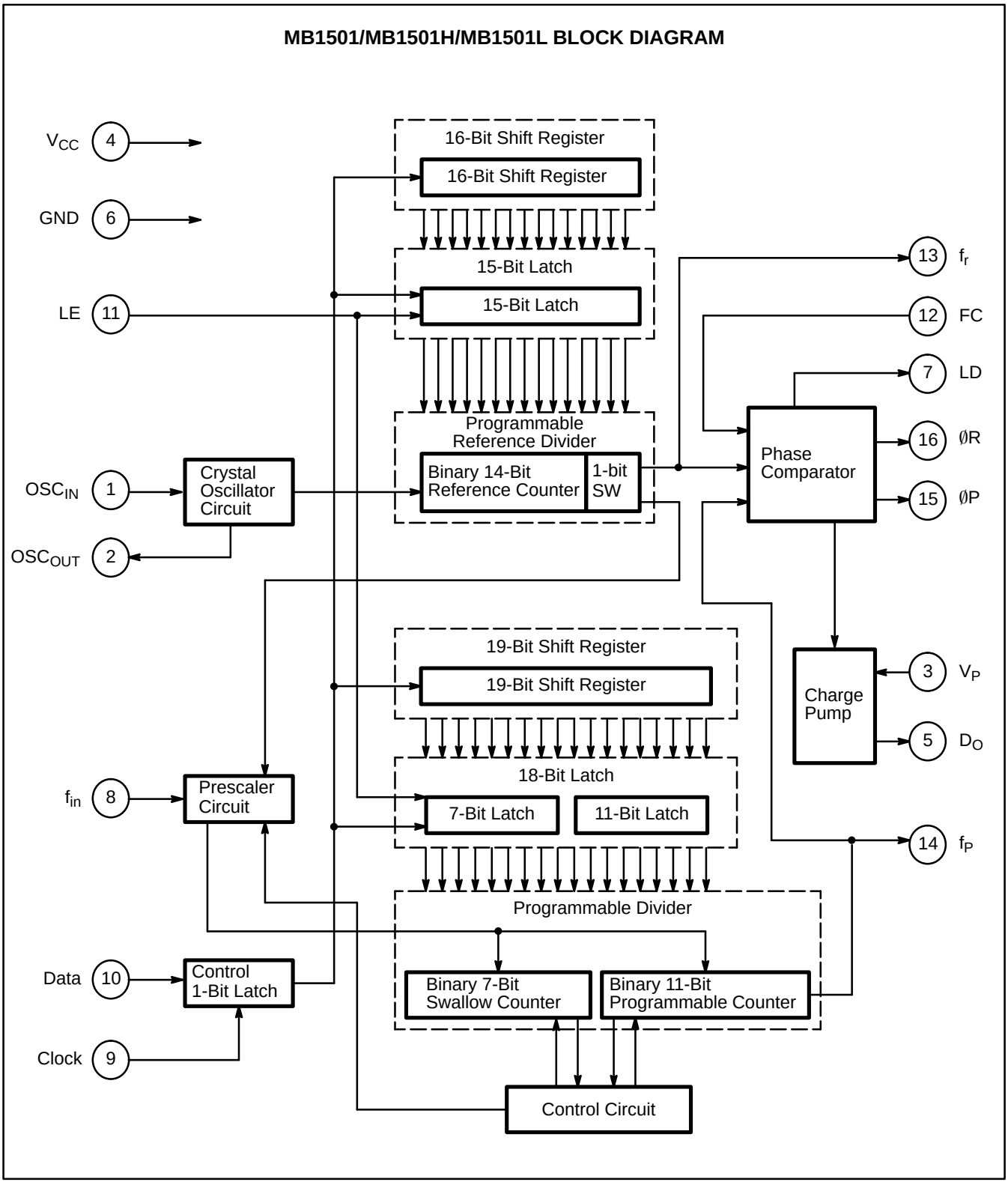
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Condition	Value	Unit
Power Supply Voltage	V_{CC}		–0.5 to +7.0	V
	V_{PH}	MB1501H	V_{CC} to 12.0	V
	V_P,V_{PL}	MB1501/1501L	V_{CC} to 10.0	
Output Voltage	V_{OUT}		–0.5 to V_{CC} +0.5	V
Open-drain Output	V_{OOPH}	MB1501H	–0.5 to 11.0	V
	V_{OOP},V_{OOPL}	MB1501/1501L	–0.5 to 9.0	
Output Current	I_{OUT}		±10	mA
Storage Temperature	T_{STG}		–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Copyright©1994 by FUJITSU LIMITED and FUJITSU MICROELECTRONICS, INC.

MB1501/MB1501H/MB1501L BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Descriptions
1 2	OSC_{IN} OSC_{OUT}	I O	Oscillator input. Oscillator output. A crystal is placed between OSC_{IN} and OSC_{OUT}.
3	V_P	—	Power supply input for charge pump.
4	V_{CC}	—	Power supply voltage input.
5	D_O	O	Charge pump output. Phase characteristic can be inversed depending upon FC input.
6	GND	—	Ground.
7	LD	O	Phase comparator output. This pin outputs high when the phase is locked. While the phase difference of f_r and f_p exists, the output level goes low.
8	f_{in}	I	Prescaler input. The connection with an external VCO should be an AC connection.
9	Clock	I	Clock input for 19-bit shift register and 16-bit shift register. Each rising edge of the clock shifts one bit of data into the shift registers.
10	Data	I	Serial data of binary code input. The last bit of the data is a control bit. The last data bit specifies which latch is activated. When the last bit is high level and LE is high-level, data is transferred to 15-bit latch. When the last bit is low level and LE is high level, data is transferred to 18-bit latch.
11	LE	I	Load enable input (with internal pull up resistor). When LE is high level (or open), data stored in the shift register is transferred to latch depending on the control data.
12	FC	O	Phase selecting input of phase comparator (with internal pull up resistor). When FC is low level, charge pump and phase detector characteristics can be inversed.
13	f_r	O	Monitor pin of phase comparator input. It is the same as programmable reference divider output.
14	f_P	O	Monitor pin of phase comparator input. It is the same as programmable divider output.
15 16	ØP ØR	O O	Outputs for external charge pump. Phase characteristics can be inversed depending on FC input. ØP pin is an N-channel open-drain output.

FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data input is input using Data pin, Clock pin and LE pin, The 15-bit programmable reference divider and 18-bit programmable divider are controlled respectively.

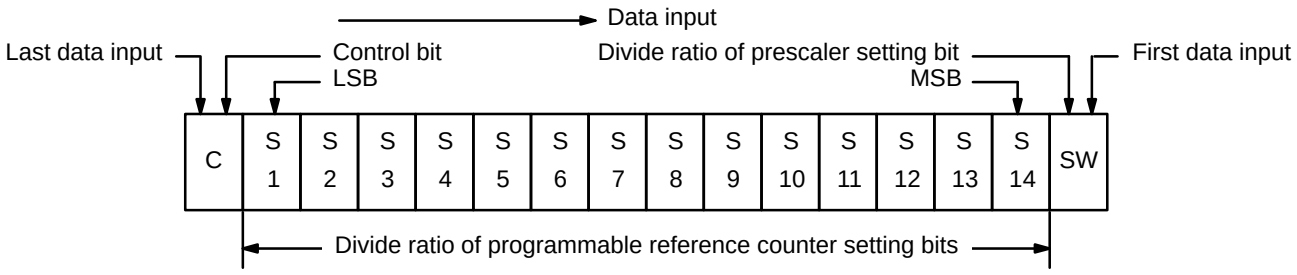
On rising edge of the clock shifts one bit of the data into the internal shift registers.

When load enable (LE) is high level (or open), data stored in shift resisters is transferred to 15-bit latch or 18-bit latch depending upon the control bit level.

Control data “H” ; Data is transferred into 15-bit latch.
Control data “L” ; Data is transferred into 18-bit latch.

PROGRAMMABLE REFERENCE DIVIDER

Programmable reference divider consists of 16-bit shift register, 15-bit latch and 14-bit reference counter. Serial 16-bit data format is shown below.



◎ 14-BIT PROGRAMMABLE REFERENCE COUNTER DIVIDE RATIO

Divide ratio R	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

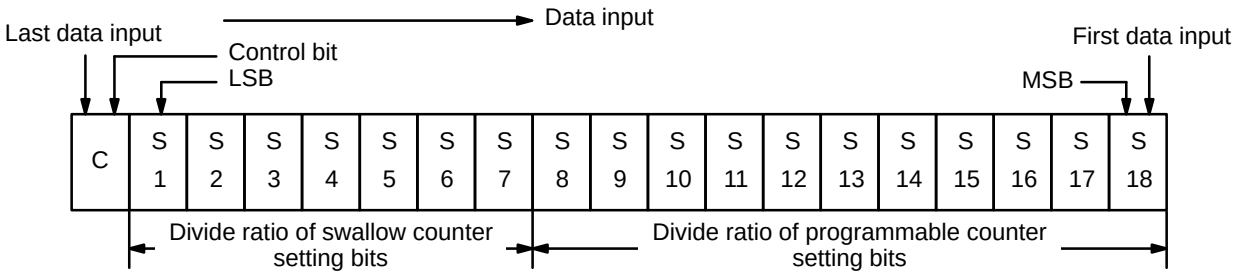
Divide ratio less than 8 is prohibited.
Divide ratio R: 8 to 16383

SW: Divide ratio of prescaler setting bit.
SW=“H” : 64
SW=“L” : 128
S_1 to S_{14}: Divide ratio of programmable reference counter setting bits (8 to 16383)
C: Control bit (Control bit is set to high.)

FUNCTIONAL DESCRIPTIONS

PROGRAMMABLE DIVIDER

Programmable divider consists of 19-bit shift register, 18-bit latch, 7-bit swallow counter and 11-bit programmable counter. Serial 19-bit data format is shown below.



◎ 7-BIT SWALLOW COUNTER DIVIDE RATIO

Divide ratio A	S7	S6	S5	S4	S3	S2	S1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

Divide ratio A : 0 to 127

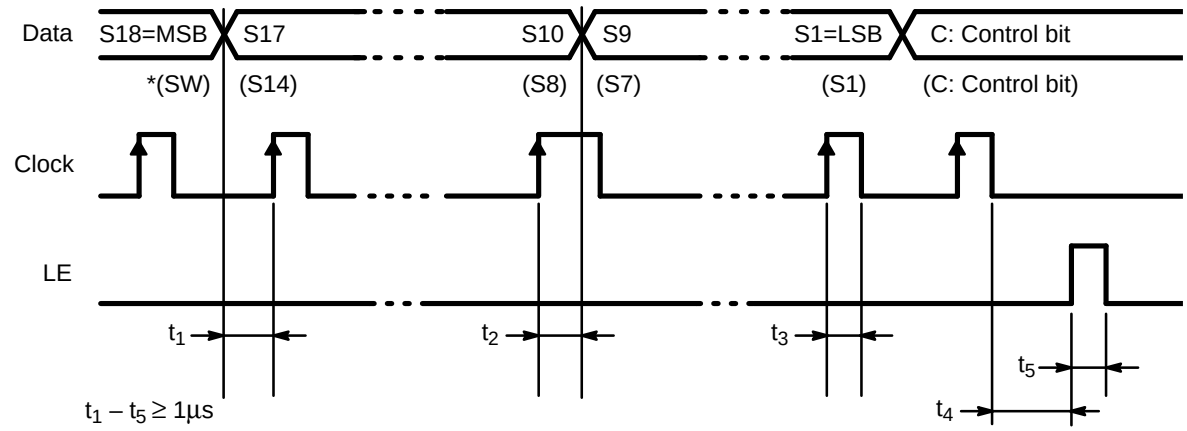
◎ 11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO

Divide ratio N	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Divide ratio less than 16 is prohibited.
Divide ratio N : 16 to 2047

S_8 to S_{18} :Divide ratio of programmable counter setting bits (16 to 2047)
S_1 to S_7 : Divide ratio of swallow counter setting bits (0 to 127)
C: Control bit (Control bit is set to low.)
Dara is input from MSB data.

SERIAL DATA INPUT TIMING



On the rising edge of the clock shifts one bit of the data into the shift registers.
Parenthsis data is used for setting the divide ratio of the programmable reference divider.

PHASE CHARACTERISTICS

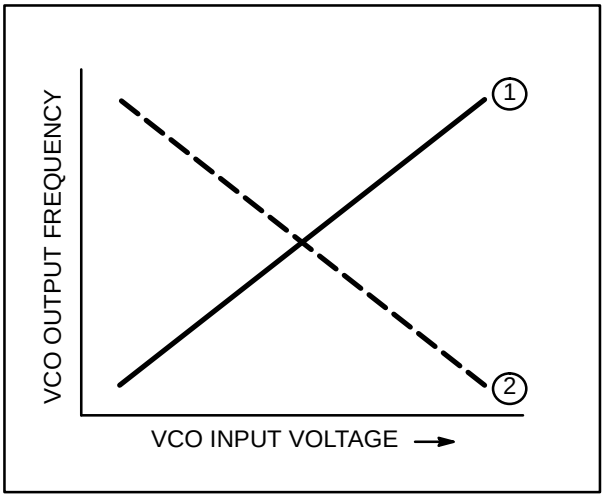
FC pin (pin 12) is provided to inverse the phase comparator characteristics. The characteristics of internal charge pump output (D_O), phase detector outputs (ØR, ØP) can be inversed depending upon FC input data. Outputs are shown below.

	FC=H (or open)			FC=L		
	D_O	ØR	ØP	D_O	ØR	ØP
$f_r > f_p$	H	L	L	L	H	Z
$f_r < f_p$	L	H	Z	H	L	L
$f_r = f_p$	Z	L	Z	Z	L	Z

Note: Z=(High impedance)

Depending upon VCO characteristics, FC pin should be set accordingly:
When VCO characteristics are like ①, FC should be set high or open circuit;
When VCO characteristics are like ②, FC should be set Low.

VCO CHARACTERISTICS



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol		Value			Unit
			Min	Typ	Max	
Power Supply Voltage	V_{CC}		2.7	3.0	5.5	V
	V_{PH}	MB1501H	V_{CC}		10.0	V
	V_P, V_{PL}	MB1501 MB1501L	V_{CC}		8.5	
Open-drain Output	V_{OOPH}	MB1501H	V_{CC}		10.0	V
	V_{OOP}, V_{OOPL}	MB1501 MB1501L	V_{CC}		8.5	
Input Voltage	V_{IN}		GND		V_{CC}	V
Operating temperature	T_A		–40		+85	°C

ELECTRICAL CHARACTERISTICS

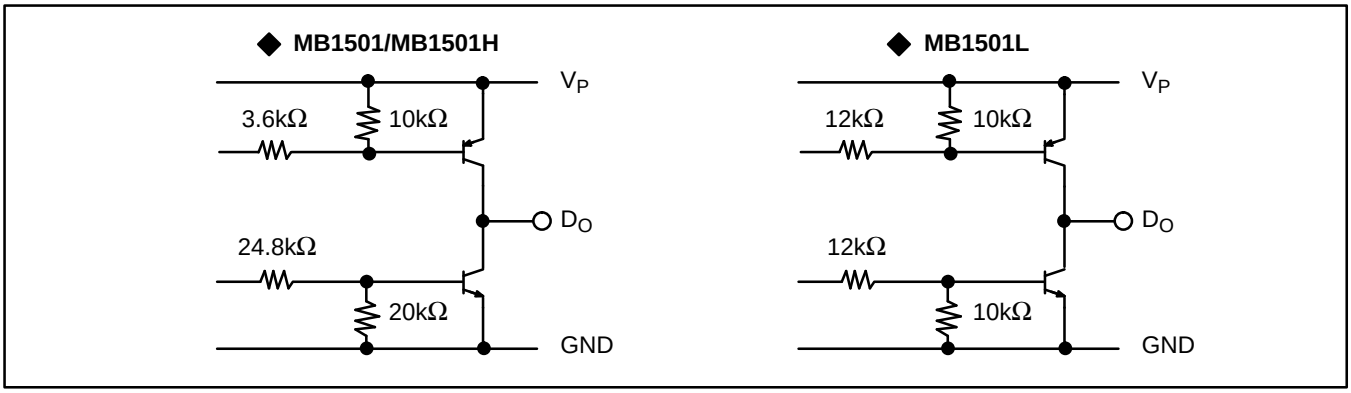
(V_{CC}=2.7 to 5.5V, T_A=–40 to +85°C)

Parameter	Pin Name	Symbol	Condition		Value			Unit
					Min	Typ	Max	
Power Supply Current	V_{CC}	I_{CC}	*1		—	15	—	mA
Operating Frequency	f_{in}	f_{IN}	*2		10	—	1100	MHz
	OSC_{IN}	f_{OSC}			—	12	20	MHz
Input Sensitivity	f_{in}	P_{fin1}	V_{CC}=2.7 to 4.0V		–10	—	6	dBm
		P_{fin2}	V_{CC}=4.0 to 5.5V		–4	—	6	dBm
	OSC_{IN}	V_{IN}			0.5	—	—	V_{P-P}
High-level Input Voltage	Except f_{in} and OSC_{IN}	V_{IH}			0.7xV_{CC}	—	—	V
Low-level Input Voltage		V_{IL}			—	—	0.3xV_{CC}	V
High-level Input Current	Data, Clock	I_{IH}			—	1.0	—	µA
Low-level Input Current		I_{IL}			—	–1.0	—	µA
Input Current	OSC_{IN}	I_{IN}			—	±50	—	µA
	LE, FC	I_{LE}			—	–60	—	µA
High-level Output Voltage	Except D_O and OSC_{OUT}	V_{OH}	V_{CC}=3.0V		2.4	—	—	V
Low-level Output Voltage		V_{OL}			—	—	0.4	V
N-channel Open-drain Cutoff Current	ØP	I_{OFF}	$V_{CC} \leq V_P \leq 8V$		—	—	1.1	µA
High-level Output Current	Except D_O and OSC_{OUT}	I_{OH}			–1.0	—	—	mA
Low-level Output Current		I_{OL}			1.0	—	—	mA
High-level Output Current	D_O	I_{DOHH}	MB1501H	V_{CC}=3V V_P=12V, T_A=25°C	–2.2	–4.5	—	mA
		I_{DOH}	MB1501	V_{CC}=3V V_P=6V, T_A=25°C	–0.5	–2.0	—	mA
		I_{DOHL}	MB1501L		–0.5	–1.1	–2.2	mA
Low-level Output Current		I_{DOLH}	MB1501H	V_{CC}=3V V_P=12V, T_A=25°C	2.2	6.0	—	mA
		I_{DOL}	MB1501	V_{CC}=3V V_P=6V, T_A=25°C	1.5	6.0	—	mA
		I_{DOLL}	MB1501L		4.5	12.0	—	mA
Leakage Current	D_O, ØP	I_{OZ}	MB1501H	V_{CC}=3V, V_P=12V T_A=25°C	—		1.0	µA
			MB1501 MB1501L	V_{CC}=3V, V_P=9V T_A=25°C				

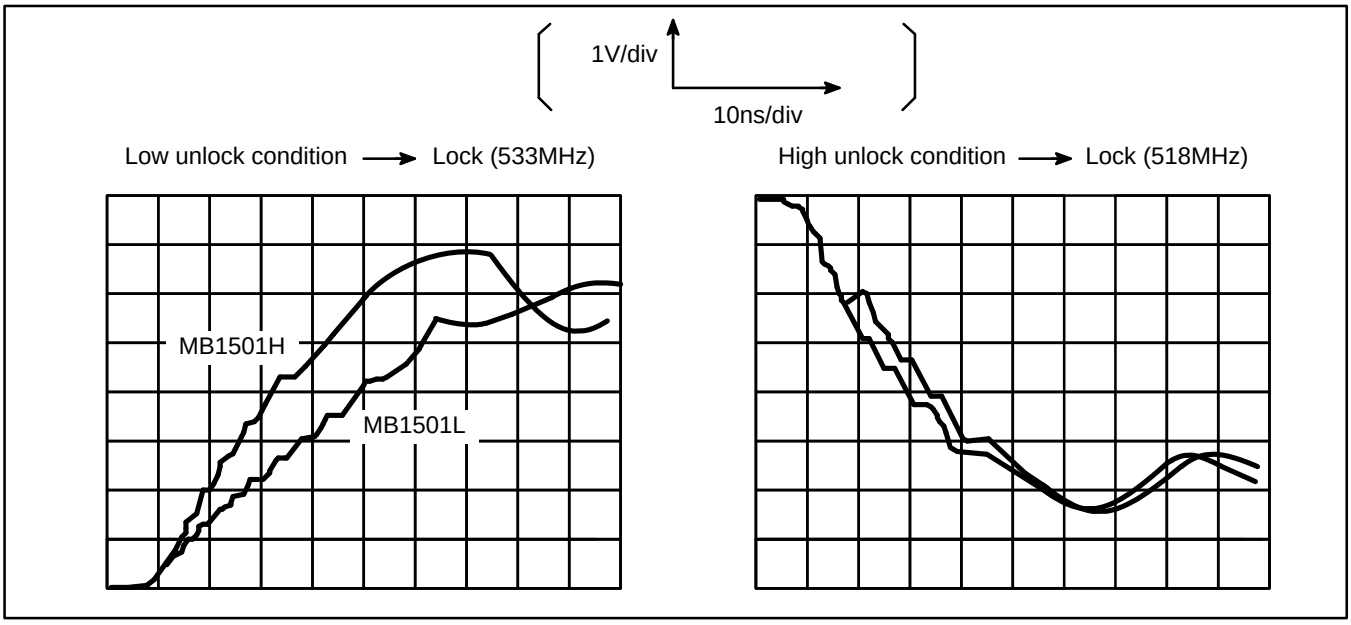
Note: *1 V_{CC}=3.0V, f_{IN}=1.1GHz, f_{OSC}=12MHz crystal.
Inputs are grounded except f_{IN}, and outputs are open.
*2 Input coupling capacitor 1000pF is connected.

TYPICAL CHARACTERISTICS CURVES

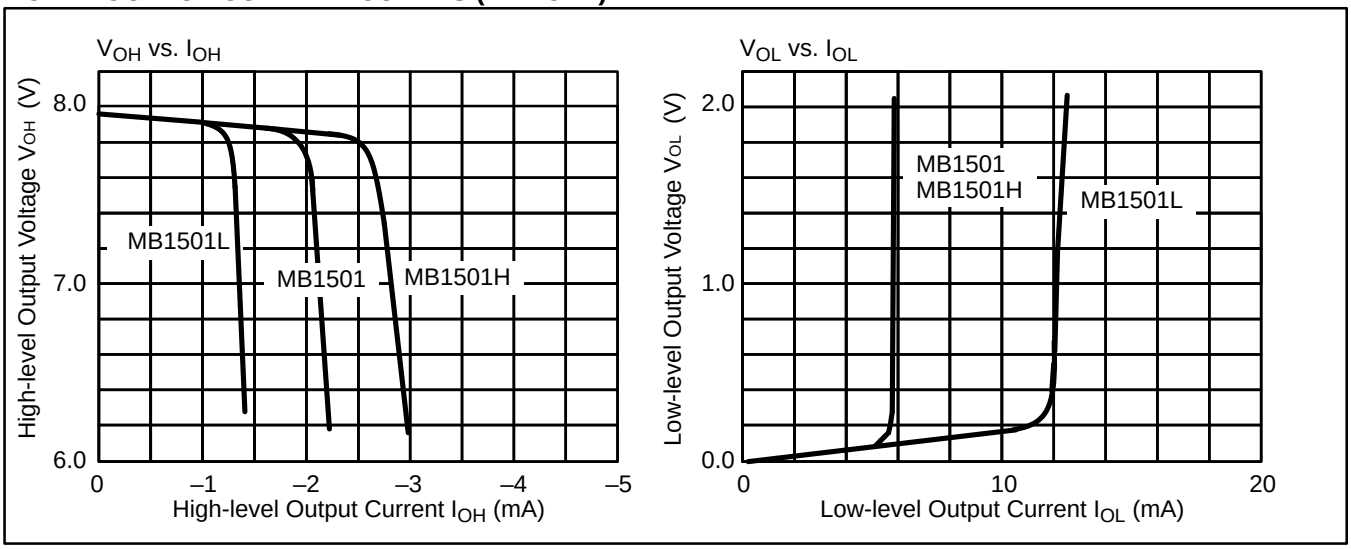
CHARGE PUMP CHARACTERISTICS



LOCK UP TIME MEASUREMENT

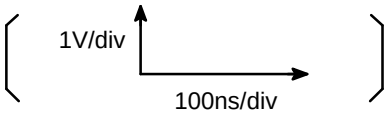


DO PIN OUTPUT CURRENT CURVES (TYPICAL)

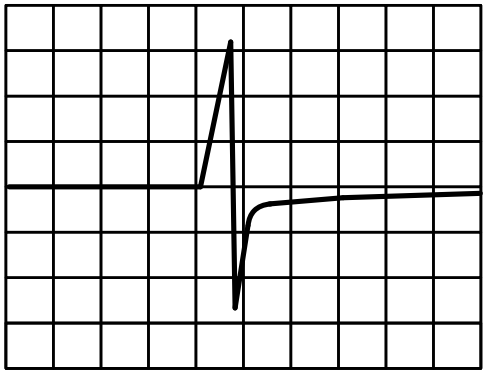


D_O PIN OUTPUT WAVEFORM AT LOCK CONDITION

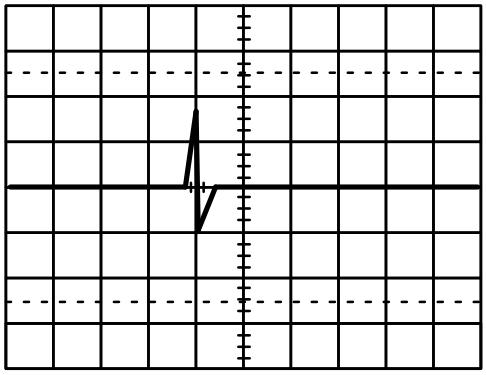
Output Waveform



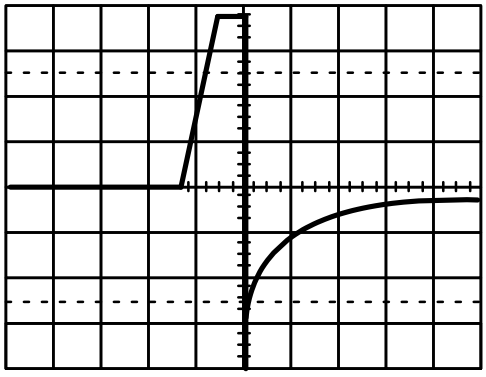
MB1501



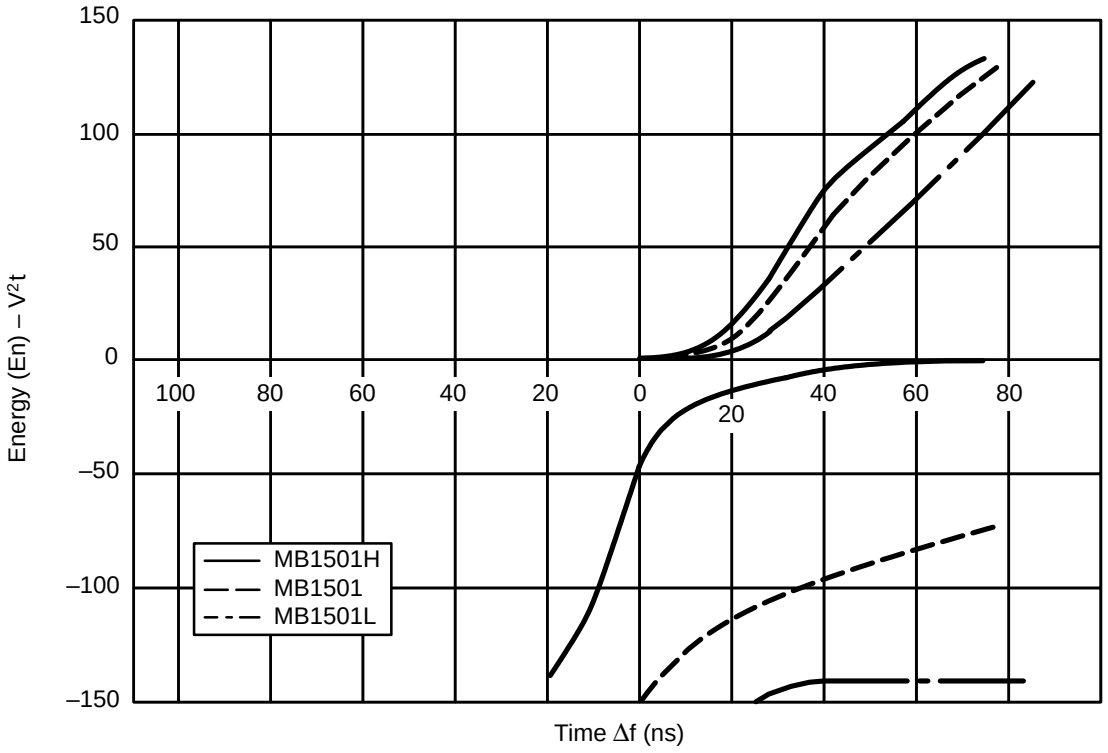
MB1501H

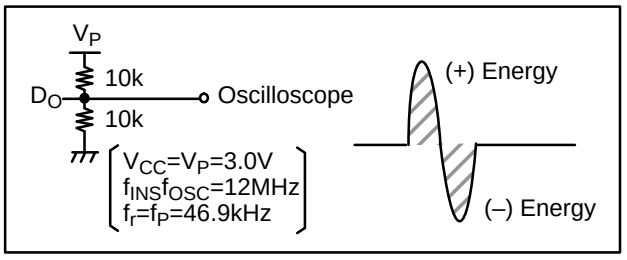


MB1501L



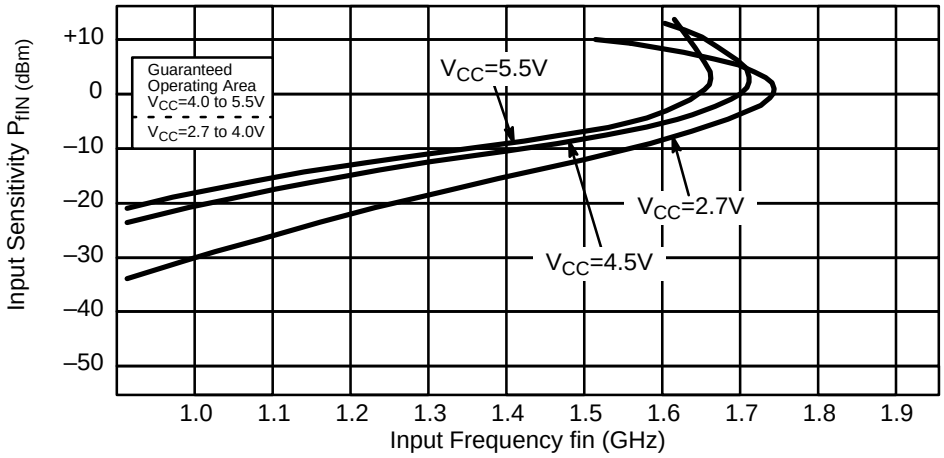
PHASE CHARACTERISTICS (Δf vs. D_O OUTPUT ENERGY)

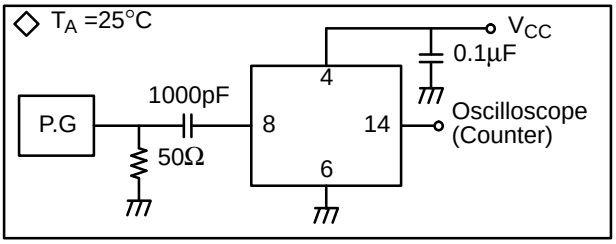




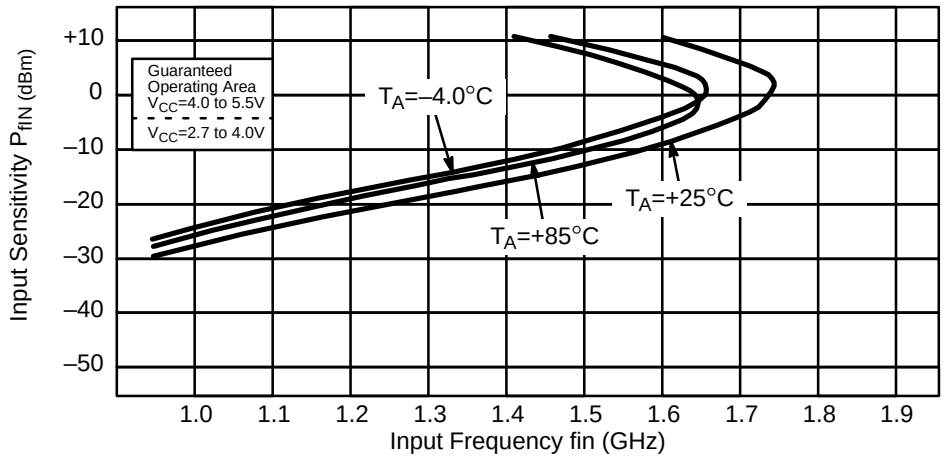
INPUT SENSITIVITY

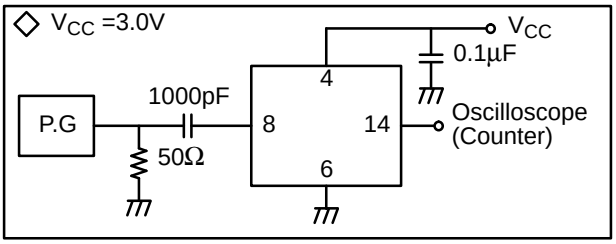
Input Sensitivity vs. Input Frequency (Supply Voltage Dependence)



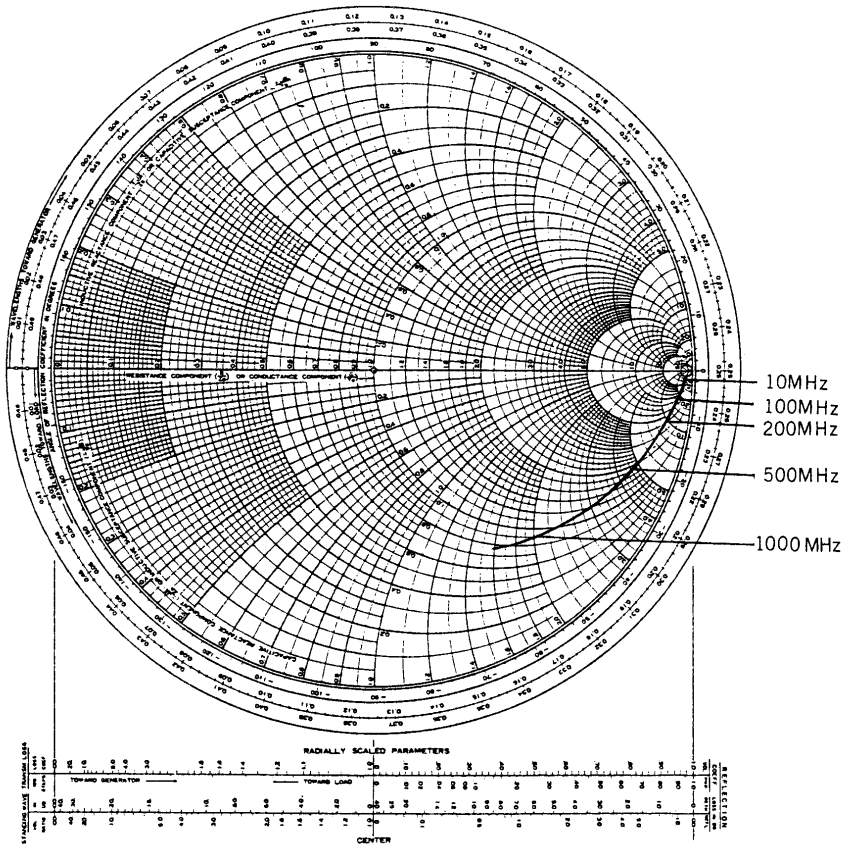


Input Sensitivity vs. Input Frequency (Temperature Dependence)



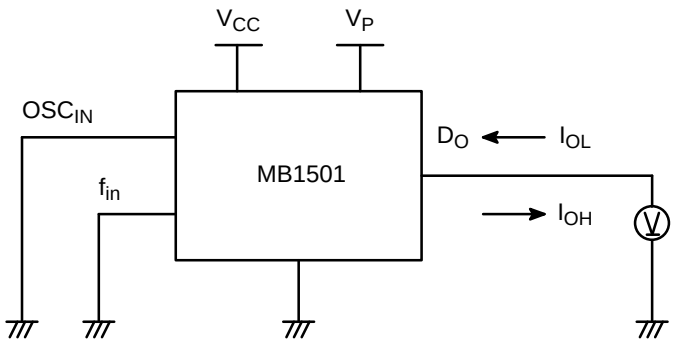


INPUT IMPEDANCE

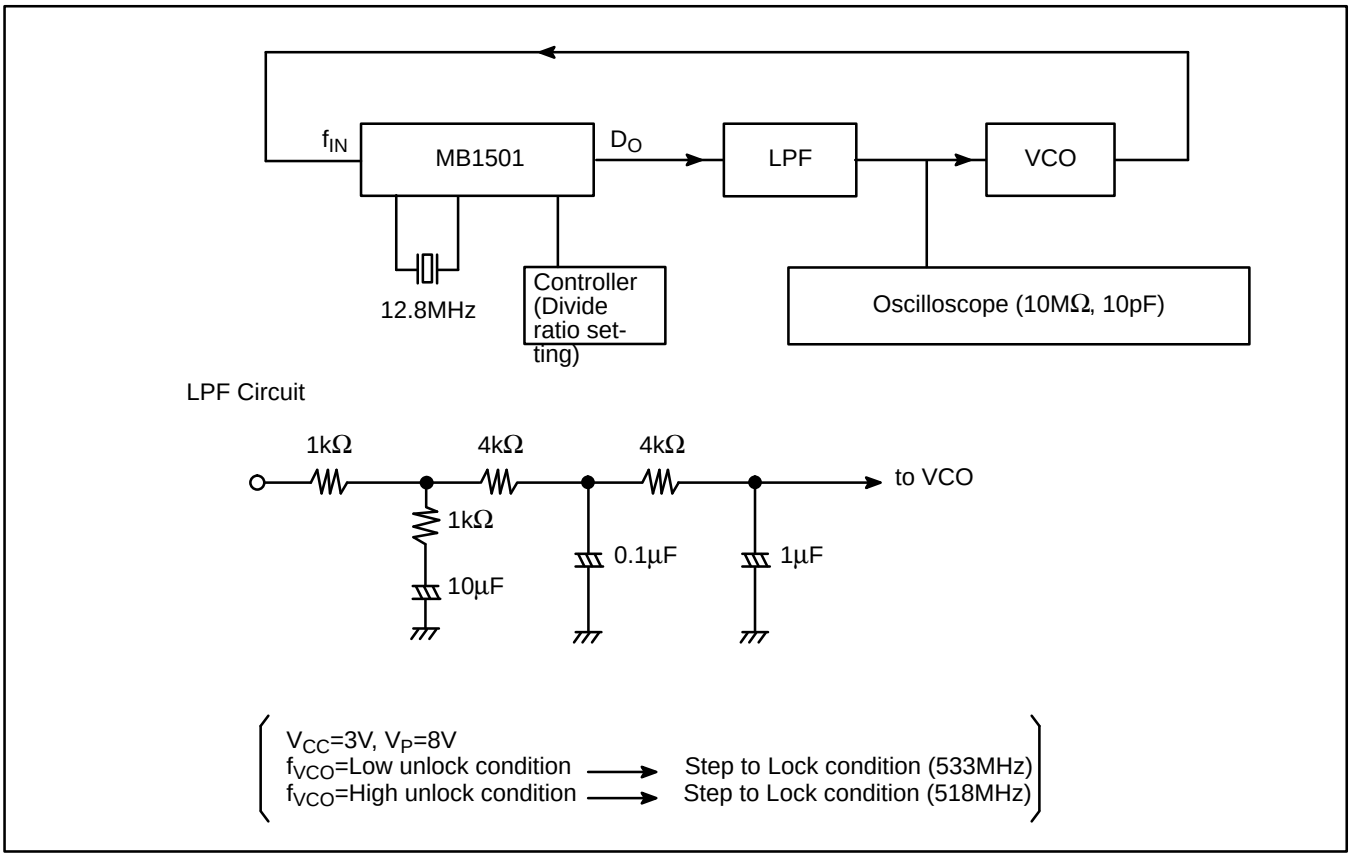


TEST CIRCUIT

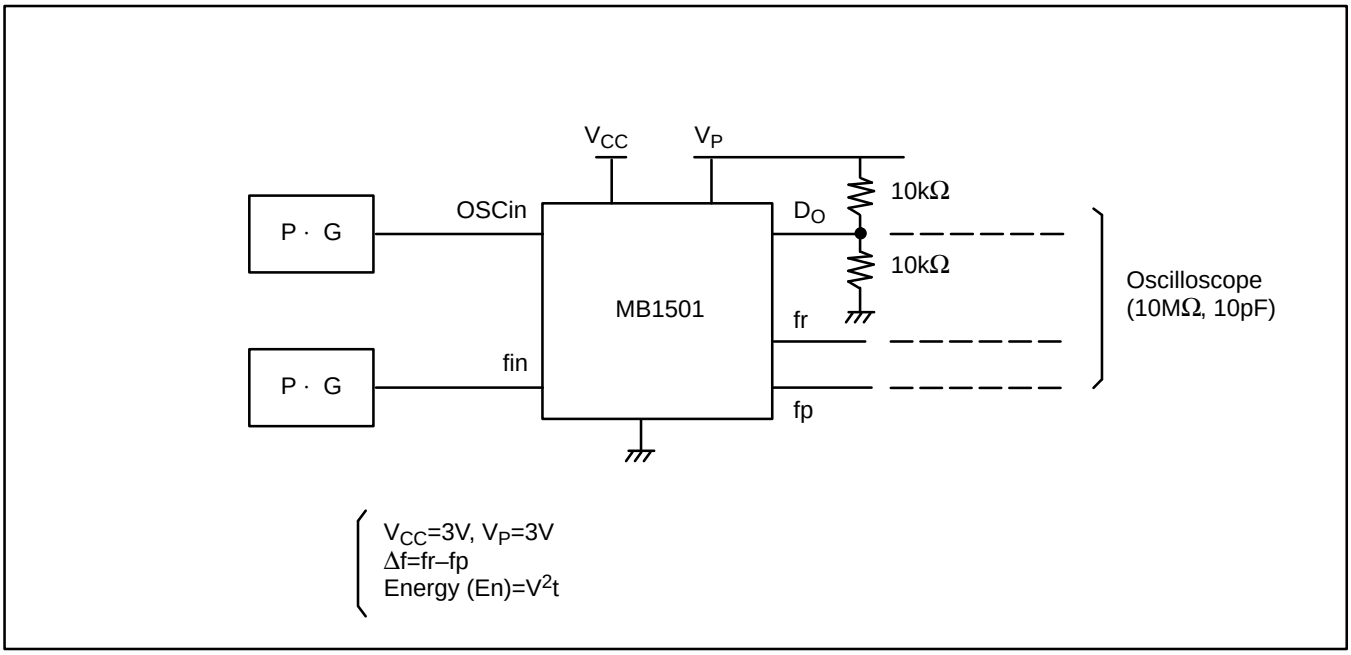
D_O Pin Output Current (I_{OH}, I_{OL}) Measurement



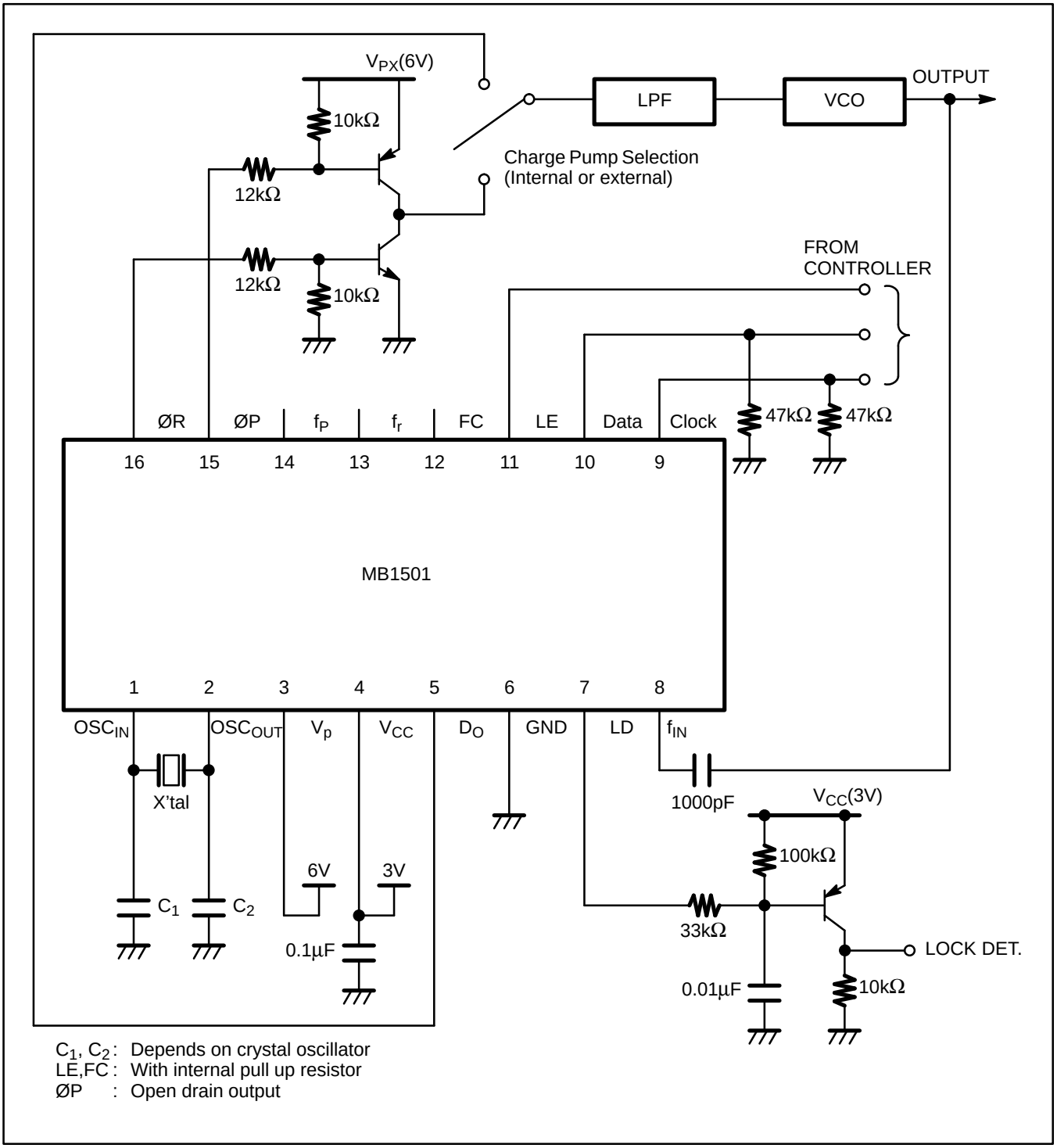
Lock up Time Measurement



Phase Characteristics Measurement



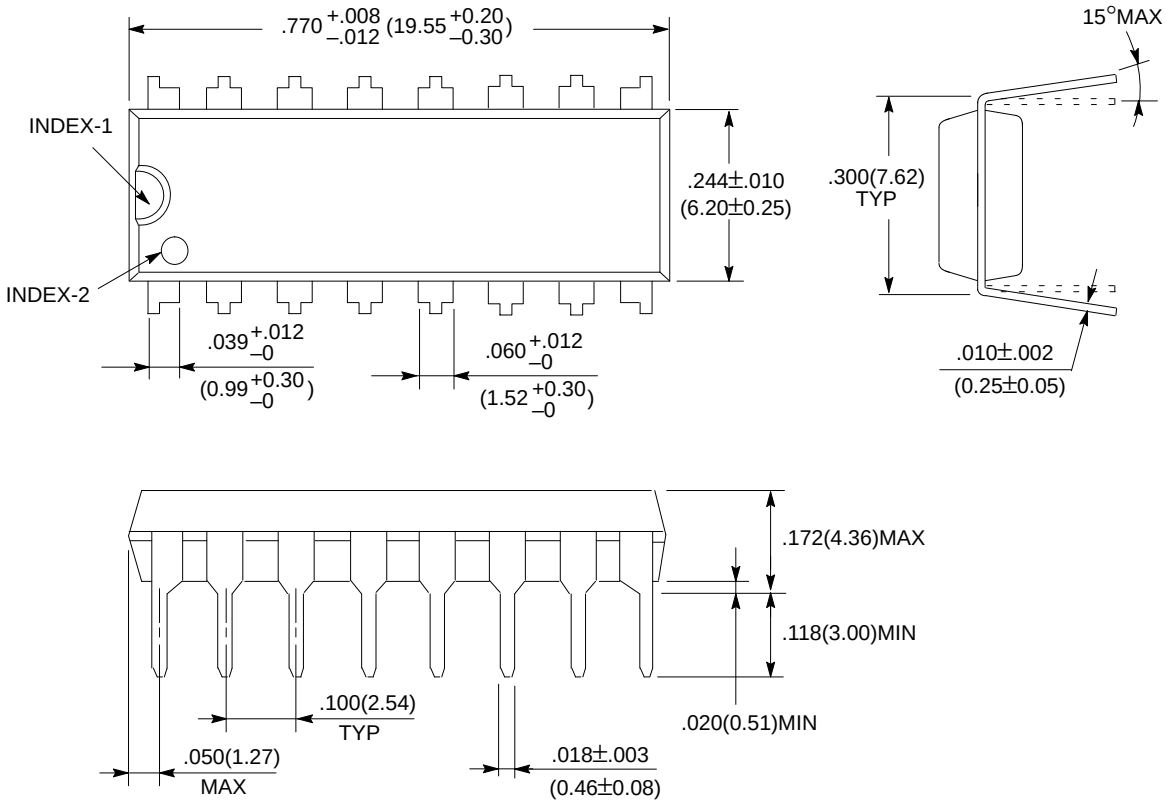
TYPICAL APPLICATION EXAMPLE



C_1, C_2 : Depends on crystal oscillator
LE,FC : With internal pull up resistor
ØP : Open drain output

PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(Case No.: DIP-16P-M04)

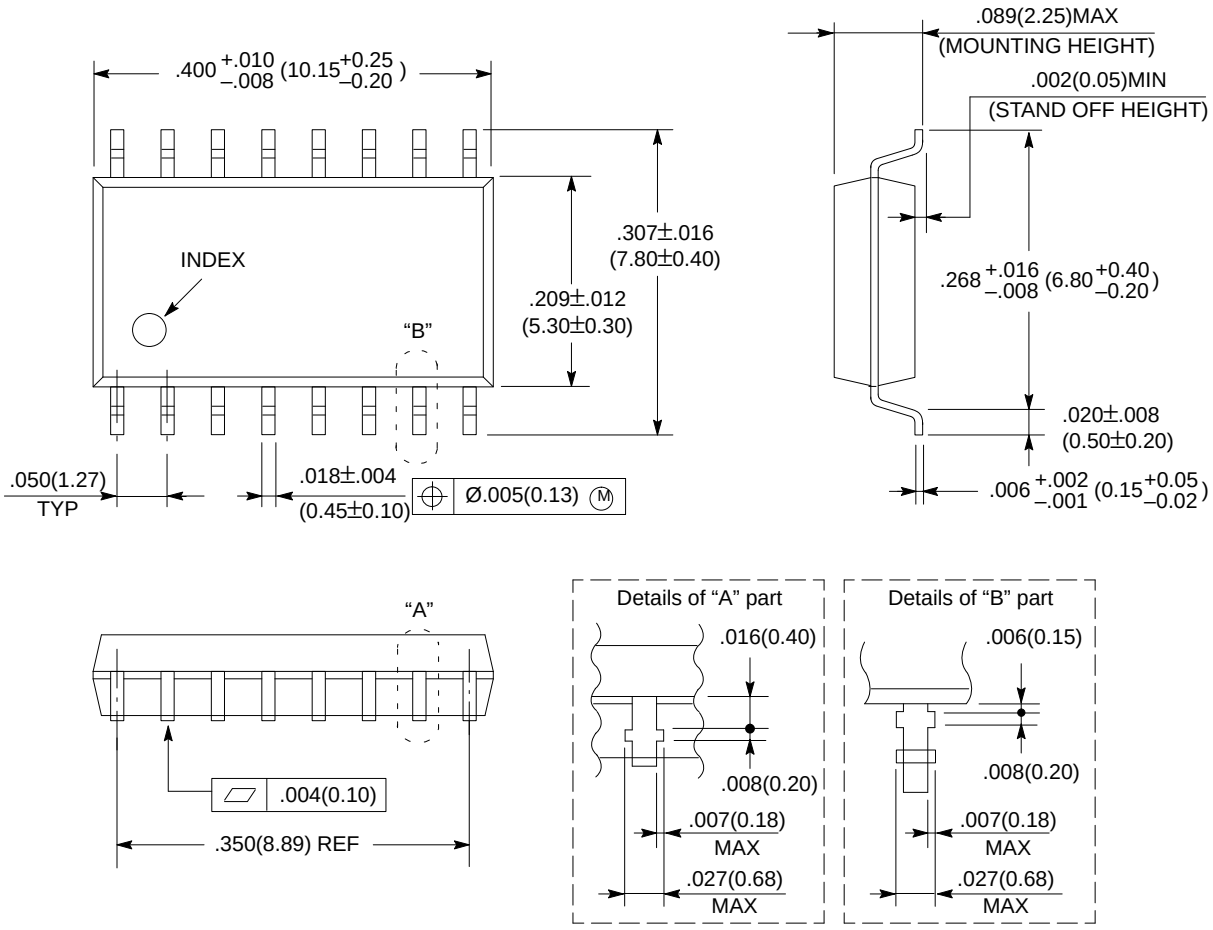


Dimensions in
inches (millimeters)

©1991 FUJITSU LIMITED D16033S-2C

PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(Case No.: FPT-16P-M06)



©1991 FUJITSU LIMITED F16015S-2C

Dimensions in
inches (millimeters)