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DS3278-1.3

NJ8821

FREQUENCY SYNTHESISER (MICROPROCESSOR INTERFACE) WITH RESETTABLE COUNTERS

The NJ8821 is a synthesiser circuit fabricated on the GPS CMOS process and is capable of achieving high sideband attenuation and low noise performance. It contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words under external control from a suitable microprocessor..

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

The NJ8821 is available in Plastic DIL (DP) and Miniature Plastic DIL (MP) packages, both with operating temperature range of −30°C to +70°C. The NJ8821MA is available only in Ceramic DIL package with operating temperature range of −40°C to +85°C.

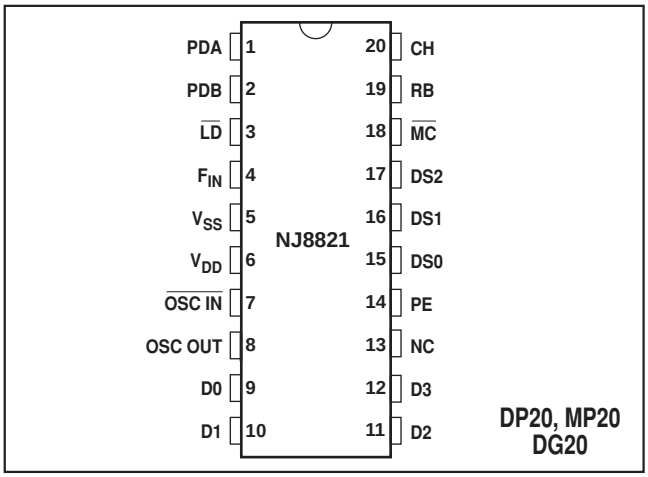


Fig.1 Pin connections - top view

FEATURES

- Low Power Consumption
- Microprocessor Compatible
- High Performance Sample and Hold Phase Detector
- >10MHz Input Frequency

ORDERING INFORMATION

NJ8821 BA DP Plastic DIL Package
NJ8821 BA MP Miniature Plastic DIL Package
NJ8821 MA DG Ceramic DIL Package

ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{DD}-V_{SS}$	−0·5V to 7V
Input voltage	
Open drain output, pin 3	7V
All other pins	$V_{SS}-0{\cdot}3V$ to $V_{DD}+0{\cdot}3V$
Storage temperature	−65°C to +150°C (DG package, NJ8821MA)
Storage temperature	−55°C to +125°C (DP and MP packages, NJ8821)

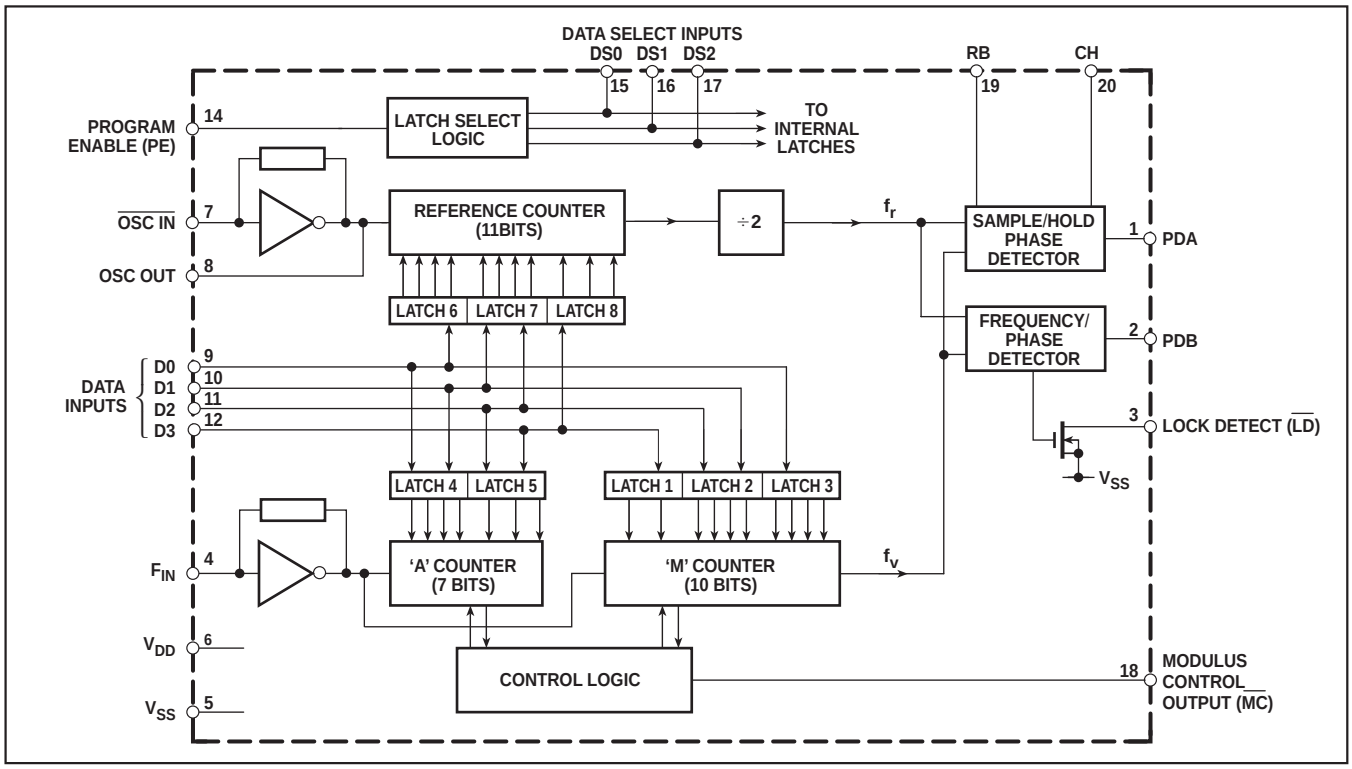


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS AT V_{DD} = 5V

Test conditions unless otherwise stated:

V_{DD}–V_{SS}=5V ±0·5V. Temperature range NJ8821 BA: –30°C to +70°C; NJ8821MA: –40°C to +85°C

DC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3·5	5·5	mA	f_{osc}, f_{FIN} = 10MHz } 0 to 5V square wave
		0·7	1·5	mA	f_{osc}, f_{FIN} = 1·0MHz }
OUTPUT LEVELS					
Modulus Control Output ($\overline{MC}$)					
High level	4·6			V	I_{SOURCE} = 1mA
Low level			0·4	V	I_{SINK} = 1mA
Lock Detect Output ($\overline{LD}$)					
Low level			0·4	V	I_{SINK} = 4mA
Open drain pull-up voltage			7	V	
PDB Output					
High level	4·6			V	I_{SOURCE} = 5mA
Low level			0·4	V	I_{SINK} = 5mA
3-state leakage current			±0·1	µA	
INPUT LEVELS					
Data Inputs (D0-D3)					
High level	4·25			V	TTL compatible
Low level			0·4	V	See note 1
Program Enable Input (PE)					
High level	4·25			V	
Low level			0·75	V	
Data Select Inputs (DS0-DS2)					
High level	4·25			V	
Low level			0·75	V	

AC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
F_{IN} and $\overline{OSC\ IN}$ input level	200			mVRMS	10MHz AC-coupled sinewave
Max. operating frequency, f_{FIN} and f_{osc}	10·6			MHz	Input squarewave V_{DD} to V_{SS}, See note 4.
Propagation delay, clock to $\overline{MC}$		30	50	ns	See note 2.
Strobe pulse width, $t_{W(ST)}$	2			µs	} See Fig. 6
Data set-up time, t_{DS}	1			µs	
Data hold time, t_{DH}	1			µs	
Latch address set-up time, t_{SE}	1			µs	
Latch address hold time, t_{HE}	1			µs	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	See note 3.
Hold capacitor, CH			1	nF	
Output resistance, PDA			5	kΩ	
Digital phase detector gain		0·4		V/Rad	

NOTES

1. Data inputs have internal pull-up resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. The finite output resistance of the internal voltage follower and 'on' resistance of the sample switch driving this pin will add a finite time constant to the loop. An external 1nF hold capacitor will give a maximum time constant of 5µs, typically.
4. Operation at up to 15MHz is possible with a full logic swing but is not guaranteed.

PIN DESCRIPTIONS

Pin no.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Output at $(V_{DD}-V_{SS})/2$ when the system is in lock. Voltage increases as f_v phase lead increases; voltage decreases as f_r phase lead increases. Output is linear over only a narrow phase window, determined by gain (programmed by RB).
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. $f_v > f_r$ or f_v leading: positive pulses with respect to the bias point V_{BIAS} $f_v < f_r$ or f_r leading: negative pulses with respect to the bias point V_{BIAS} $f_v = f_r$ and phase error within PDA window: high impedance.
3	$\overline{LD}$	An open-drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
4	F_{IN}	The input to the main counters, normally driven from a prescaler, which may be AC-coupled or, when a full logic swing is available, may be DC-coupled.
5	V_{SS}	Negative supply (ground).
6	V_{DD}	Positive supply.
7, 8	$\overline{OSC\ IN}$/ OSC OUT	These pins form an on-chip reference oscillator when a series resonant crystal is connected across them. Capacitors of appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external reference signal may, alternatively, be applied to $\overline{OSC\ IN}$. This may be a low-level signal, AC-coupled, or if a full logic swing is available it may be DC-coupled. The program range of the reference counter is 3 to 2047, with the division ratio being twice the programmed number.
9,10, 11, 12	D0-D3	Data on these inputs is transferred to the internal data latches during the appropriate data read time slot. D3 is MSB, D0 is LSB.
13	NC	No connection
14	PE	This pin is used as a strobe for the data. A logic '1' on this pin transfers data from the D0-D3 pins to the internal latch addressed by the data select (DS0-DS2) pins . A logic '0' disables the data inputs.
15, 16, 17	DS0-DS2	Data select inputs for addressing the internal data latches
18	$\overline{MC}$	Modulus control output for controlling an external dual-modulus prescaler. $\overline{MC}$ will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. $\overline{MC}$ then goes high and remains high until the 'M' counter completes its cycle, at which point both 'A' and 'M' counters are reset. This gives a total division ratio of $MP+A$, where P and $P+1$ represent the dual-modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The programming range of the 'M' counter is 8-1023 and, for correct operation, $M \geqslant A$. Where every possible channel is required, the minimum total division ratio should be P^2-P.
19	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
20	CH	An external hold capacitor should be connected between this pin and V_{SS}.

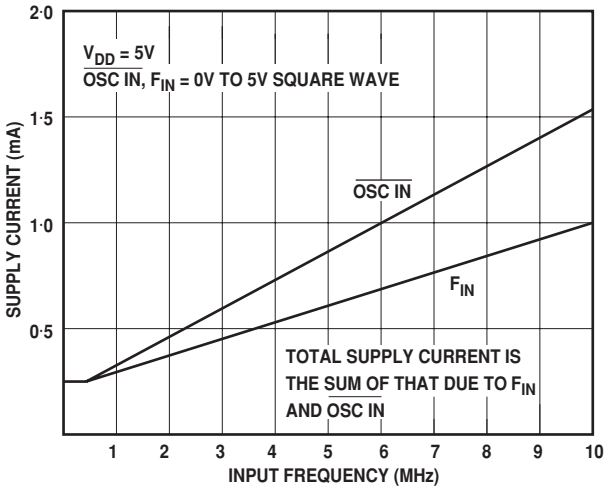


Fig. 3 Typical supply current v. input frequency

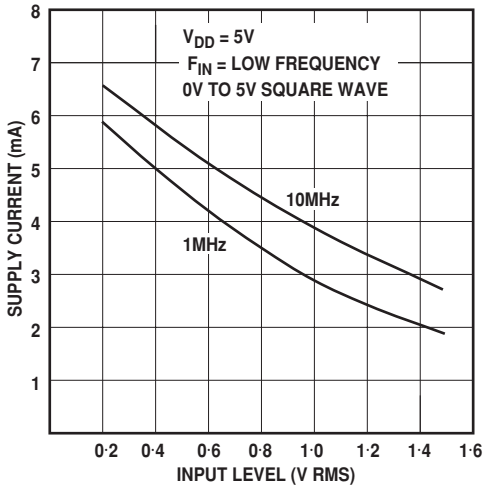


Fig. 4 Typical supply current v. input level, $\overline{OSC\ IN}$

PROGRAMMING

Timing is generated externally, normally from a microprocessor, and allows the user to change the data in selected latches as defined by the data map Fig.5. The PE pin is used as a strobe for the data: taking PE high causes data to be transferred from the data pins (D0-D3) into the addressed latch. Following the falling edge of PE, the data is retained in the addressed latch and the data inputs are disabled. Data transfer from all internal latches into the counters occurs simultaneously with the transfer of data into latch 1, which would therefore normally be the last latch addressed during each channel change. Timing information for this mode of operation is given in Fig. 6.

When re-programming, a reset to zero state is followed by reloading with the new counter values. This means that the synthesiser loop lock-up time is well defined and less than 10ms. If shorter lock-up times are are required when making only small changes in frequency, the GPS NJ8823 (with non-resettable counters) should be considered.

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig. 5 Data map

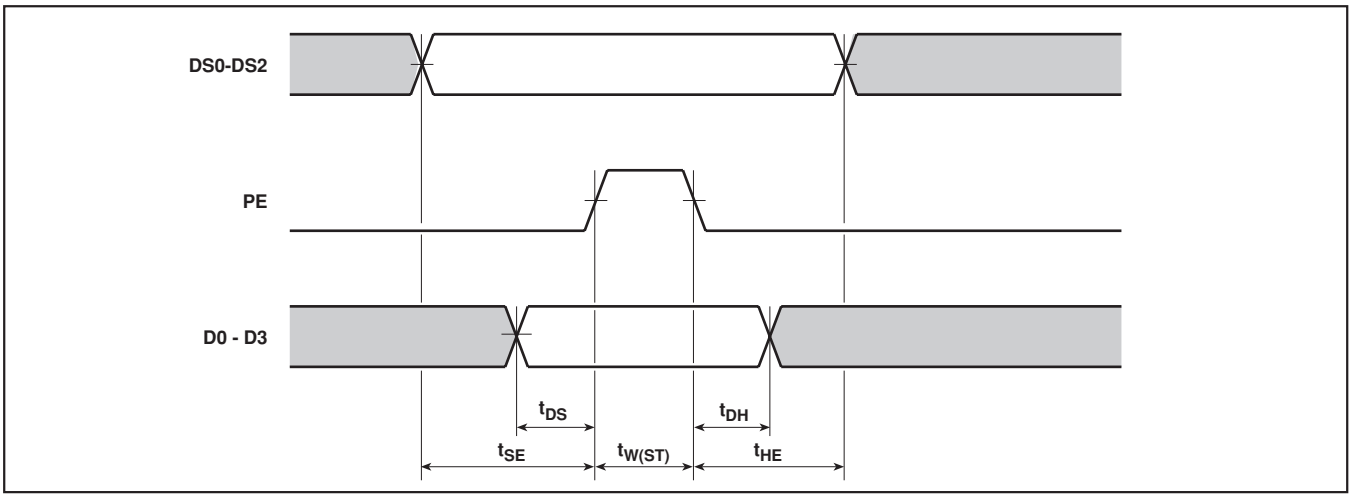


Fig. 6 Timing diagram

PHASE COMPARATORS

The digital phase/frequency detector drives a three-state output, PDB, which provides a 'coarse' error signal to enable fast switching between channels. The PDB output is active until the phase error is within the sample and hold phase detector, PDA, window, when PDB becomes high impedance. Phase-lock is indicated at this point by a low level on $\overline{LD}$. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp, controlled by the digital output from both the reference and main divider chains, is sampled at the reference frequency to give the 'fine' error signal, PDA. When in phase lock, this output would be typically at $(V_{DD}-V_{SS})/2$ and any offset from this would be proportional to phase error. The relationship between this offset and the phase error is the phase comparator gain, which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the inclusion of a resistor between pin 8 (OSC OUT) and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

Data and signal input pins should not have input applied to them prior to the application of V_{DD}, as otherwise latch-up may occur.

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