DATA SHEET



TDA6650TT; TDA6651TT

5 V mixer/oscillator and low noise PLL synthesizer for hybrid terrestrial tuner (digital and analog)

Product specification
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PHILIPS

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5 V mixer/oscillator and low noise PLL synthesizer for hybrid terrestrial tuner (digital and analog)

TDA6650TT; TDA6651TT

1 FEATURES

- Single-chip 5 V mixer/oscillator and low phase noise PLL synthesizer for TV and VCR tuners, dedicated to hybrid (digital and analog) as well as pure digital applications (DVB-T)
- Five possible step frequencies to cope with different digital terrestrial TV and analog TV standards
- Eight charge pump currents between 40 and 600 μA to reach the optimum phase noise performance over the bands
- Automatic Loop Bandwidth Control (ALBC) sets the optimum phase noise performance for DVB-T channels
- I^2C-bus protocol compatible with 2.5, 3.3 and 5 V microcontrollers:
  - Address + 5 data bytes transmission (I^2C-bus write mode)
  - Address + 1 status byte (I^2C-bus read mode)
  - Four independent I^2C-bus addresses
- Five PMOS open-drain ports with 15 mA source capability for band switching and general purpose; one of these ports is combined with a 5-step ADC
- Wide band AGC detector for internal tuner AGC:
  - Six programmable take-over points
  - Two programmable time constants
  - AGC flag
- In-lock flag
- Crystal frequency output buffer
- 33 V tuning voltage output
- Fractional-N programmable divider
- Balanced mixers with a common emitter input for the low band and for the mid band (each single input)
- Balanced mixer with a common base input for the high band (balanced input)
- 2-pin asymmetrical oscillator for the low band
- 2-pin symmetrical oscillator for the mid band
- 4-pin symmetrical oscillator for the high band
- Switched concept IF amplifier with both asymmetrical and symmetrical outputs to drive low impedance or SAW filters i.e. 500 Ω//40 pF.

2 APPLICATIONS

- Digital and analog terrestrial tuners (OFDM, PAL, etc.)
- Cable tuners (QAM)
- Digital TV sets
- Digital set-top boxes.

3 GENERAL DESCRIPTION

The TDA6650TT; TDA6651TT is a programmable 3-band mixer/oscillator and low phase noise PLL synthesizer intended for pure 3-band tuner concepts applied to hybrid (digital and analog) terrestrial and cable TV reception.

The device includes three double balanced mixers for low, mid and high bands, three oscillators for the corresponding bands, a switchable IF amplifier, a wide band AGC detector and a low noise PLL synthesizer. The frequencies of the three bands are shown in Table 1. Two pins are available between the mixer output and the IF amplifier input to enable IF filtering for improved signal handling and to improve the adjacent channel rejection.

Table 1 Recommended band limits in MHz for PAL and DVB-T tuners; note 1

BAND	RF INPUT		OSCILLATOR	
	MIN.	MAX.	MIN.	MAX.
Low	44.25	157.25	83.15	196.15
Mid	157.25	443.25	196.15	482.15
High	443.25	863.25	482.15	902.15

Note

1. RF input frequency is the frequency of the corresponding picture carrier for analog standard.

The IF amplifier is switchable in order to drive both symmetrical and asymmetrical outputs. When it is used as an asymmetrical amplifier, the IFOUTB pin needs to be connected to the supply voltage V_{CCA}.

Five open-drain PMOS ports are included on the IC. Two of them, BS1 and BS2, are also dedicated to the selection of the low, mid and high bands. PMOS port BS5 pin is shared with the ADC.

The AGC detector provides a control that can be used in a tuner to set the gain of the RF stage. Six AGC take-over points are available by software. Two programmable AGC time constants are available for search tuning and normal tuner operation.

The local oscillator signal is fed to the fractional-N divider. The divided frequency is compared to the comparison frequency into the fast phase detector which drives the charge pump. The loop amplifier is also on-chip, including the high-voltage transistor to drive directly the 33 V tuning voltage without the need to add an external transistor.

The comparison frequency is obtained from an on-chip crystal oscillator. The crystal frequency can be output to the XTOUT pin to drive the clock input of a digital demodulation IC.

Control data is entered via the I^2C-bus; six serial bytes are required to address the device, select the local oscillator (LO) frequency, select the step frequency, program the output ports and set the charge pump current or select the ALBC mode, enable or disable the crystal output buffer, select the AGC take-over point and time constant and/or select a specific test mode. A status byte concerning the AGC level detector and the ADC voltage can be read out on the SDA line during a read operation. During a read operation, the loop ‘in-lock’ flag, the Power-on reset flag and the automatic loop bandwidth control flag are read.

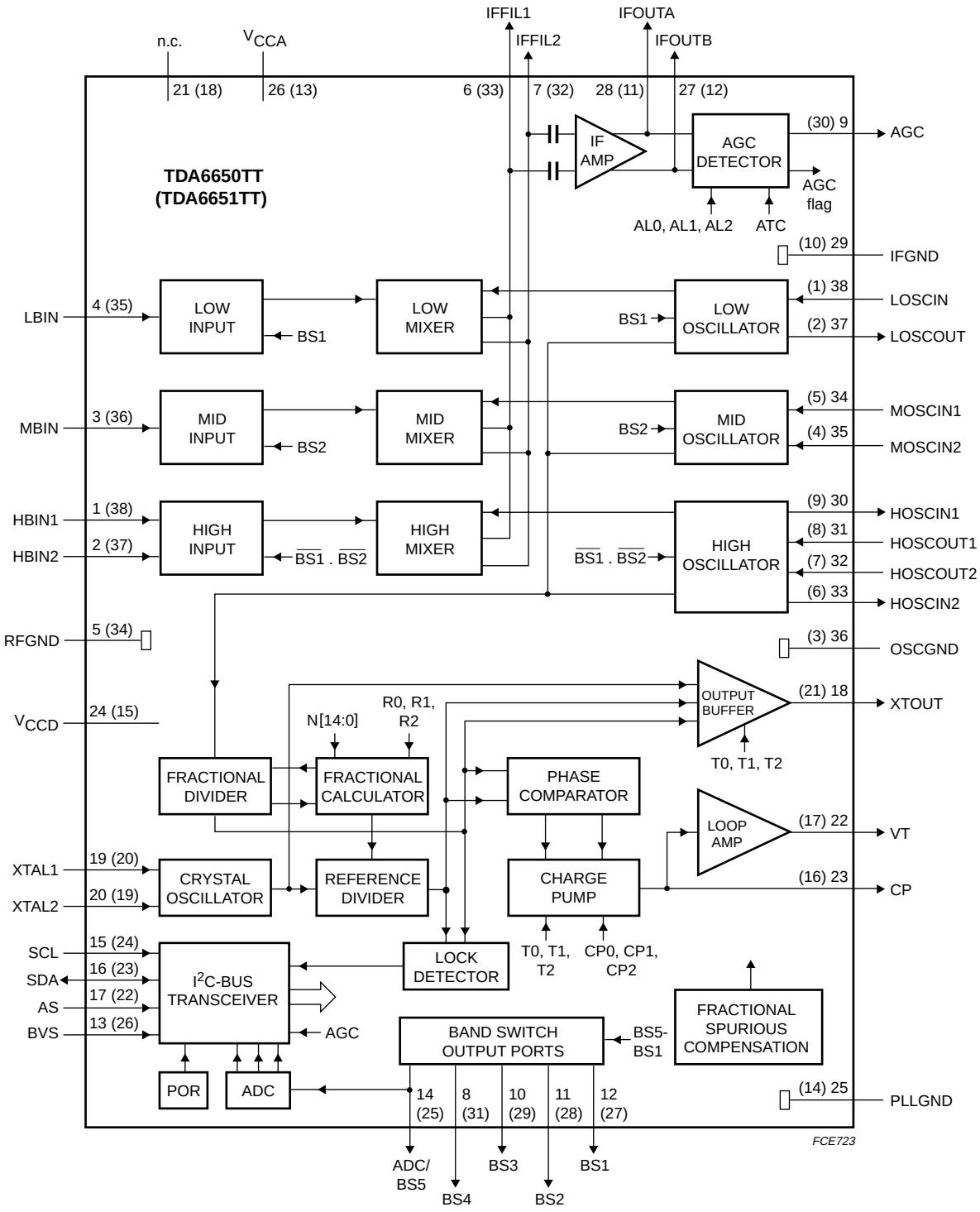
The device has 4 programmable addresses. Each address can be selected by applying a specific voltage to pin AS, enabling the use of multiple devices in the same system.

The I^2C-bus is fast mode compatible, except for the timing as described in the functional description and is compatible with 5, 3.3 and 2.5 V microcontrollers depending on the voltage applied to pin BVS.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA6650TT	TSSOP38	plastic thin shrink small outline package; 38 leads; body width 4.4 mm; lead pitch 0.5 mm	SOT510-1
TDA6651TT			

5 BLOCK DIAGRAM



The pin numbers in parenthesis represent the TDA6651TT.

Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN		DESCRIPTION
	TDA6650TT	TDA6651TT	
HBIN1	1	38	high band RF input 1
HBIN2	2	37	high band RF input 2
MBIN	3	36	mid band RF input
LBIN	4	35	low band RF input
RFGND	5	34	RF ground
IFFIL1	6	33	IF filter output 1
IFFIL2	7	32	IF filter output 2
BS4	8	31	PMOS open-drain output port 4 for general purpose
AGC	9	30	AGC output
BS3	10	29	PMOS open-drain output port 3 for general purpose
BS2	11	28	PMOS open-drain output port 2 to select the mid band
BS1	12	27	PMOS open-drain output port 1 to select the low band
BVS	13	26	bus voltage selection input
ADC/BS5	14	25	ADC input or PMOS open-drain output port 5 for general purpose
SCL	15	24	I^2C-bus serial clock input
SDA	16	23	I^2C-bus serial data input and output
AS	17	22	I^2C-bus address selection input
XTOUT	18	21	crystal frequency buffer output
XTAL1	19	20	crystal oscillator input 1
XTAL2	20	19	crystal oscillator input 2
n.c	21	18	not connected
VT	22	17	tuning voltage output
CP	23	16	charge pump output
V_{CCD}	24	15	supply voltage for the PLL part
PLLGND	25	14	PLL ground
V_{CCA}	26	13	supply voltage for the analog part
IFOUTB	27	12	IF output B for symmetrical amplifier and asymmetrical IF amplifier switch input
IFOUTA	28	11	IF output A
IFGND	29	10	IF ground
HOSCIN1	30	9	high band oscillator input 1
HOSCOUT1	31	8	high band oscillator output 1
HOSCOUT2	32	7	high band oscillator output 2
HOSCIN2	33	6	high band oscillator input 2
MOSCIN1	34	5	mid band oscillator input 1
MOSCIN2	35	4	mid band oscillator input 2
OSCGND	36	3	oscillators ground
LOSCOUT	37	2	low band oscillator output
LOSCIN	38	1	low band oscillator input

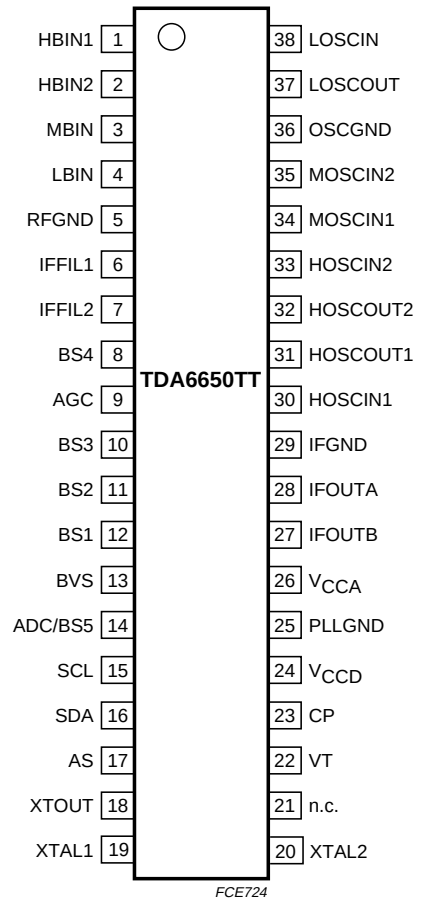


Fig.2 Pin configuration TDA6650TT.

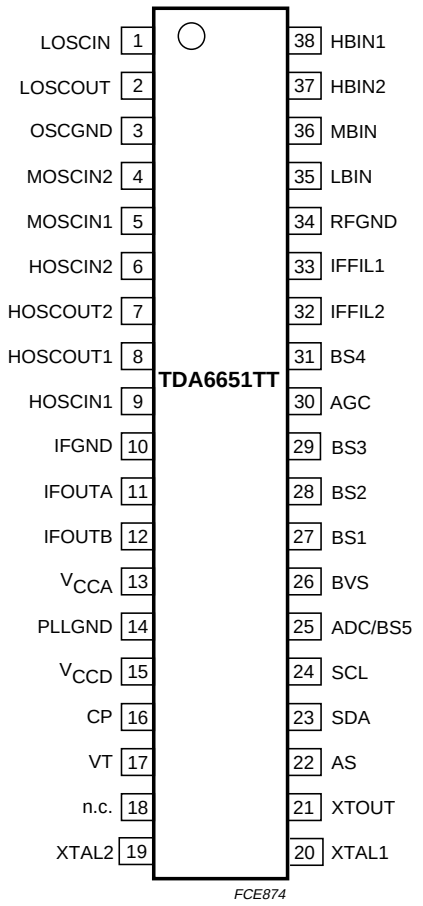


Fig.3 Pin configuration TDA6651TT.

7 FUNCTIONAL DESCRIPTION

7.1 Mixer, Oscillator and PLL (MOPLL) functions

Bit BS1 enables the BS1 port, the low band mixer and the low band oscillator. Bit BS2 enables the BS2 port, the mid band mixer and the mid band oscillator. When both BS1 and BS2 bits are logic 0, the high band mixer and the high band oscillator are enabled.

The oscillator signal is applied to the fractional-N programmable divider. The divided signal f_{div} is fed to the phase comparator where it is compared in both phase and frequency with the comparison frequency f_{comp}. This frequency is derived from the signal present on the crystal oscillator f_{xtal} and divided in the reference divider. There is a fractional calculator on the chip that generates the data for the fractional divider as well as the reference divider ratio, depending on the step frequency selected. The crystal oscillator requires a 4 MHz crystal in series with an 18 pF capacitor between pins XTAL1 and XTAL2.

The output of the phase comparator drives the charge pump and the loop amplifier section. This amplifier has an on-chip high voltage drive transistor. Pin CP is the output of the charge pump, and pin VT is the pin to drive the tuning voltage to the varicap diodes of the oscillators and the tracking filters. The loop filter has to be connected between pins CP and VT. The spurious signals introduced by the fractional divider are automatically compensated by the spurious compensation block.

It is possible to drive the clock input of a digital demodulation IC from pin XTOUT with the 4 MHz signal from the crystal oscillator. This output is also used to output $^1/_2 f_{div}$ and f_{comp} signals in a specific test mode (see Table 6). It is possible to switch off this output, which is recommended when it is not used.

For test and alignment purposes, it is also possible to release the tuning voltage output by selecting the sinking mode (see Table 6), and by applying an external voltage on pin VT.

In addition to the BS1 and BS2 output ports that are used for the band selection, there are three general purpose ports BS3, BS4 and BS5. All five ports are PMOS open-drain type, each with 15 mA drive capability. The connection for port BS5 and the ADC input is combined on one pin. It is not possible to use the ADC if port BS5 is used.

The AGC detector compares the level at the IF amplifier output to a reference level which is selected from 6 different levels via the I²C-bus. The time constant of the AGC can be selected via the I²C-bus to cope with normal operation as well as with search operation.

When the output level on pin AGC is higher than the threshold V_{RMH}, then bit AGC = 1. When the output level on pin AGC is lower than the threshold V_{RML}, then bit AGC = 0. Between these two thresholds, bit AGC is not defined. The status of the AGC bit can be read via the I²C-bus according to the read mode as described in Table 12.

7.2 I²C-bus voltage

The I²C-bus lines SCL and SDA can be connected to an I²C-bus system tied to 2.5, 3.3 or 5 V. The choice of the bus input threshold voltages is made with pin BVS that can be left open-circuit, connected to the supply voltage or to ground (see Table 2).

Table 2 I²C-bus voltage selection

PIN BVS CONNECTION	BUS VOLTAGE	LOGIC LEVEL	
		LOW	HIGH
To ground	2.5 V	0 to 0.75 V	1.75 to 5.5 V
Open-circuit	3.3 V	0 to 1.0 V	2.3 to 5.5 V
To V_{CC}	5 V	0 to 1.5 V	3.0 to 5.5 V

7.3 Phase noise, I²C-bus traffic and crosstalk

While the TDA6650TT; TDA6651TT is dedicated for hybrid terrestrial applications, the low noise PLL will clean up the noise spectrum of the VCOs close to the carrier to reach noise levels at 1 kHz offset from the carrier compatible with e.g. DVB-T reception.

Linked to this noise improvement, some disturbances may become visible while they were not visible because they were hidden into the noise in analog dedicated applications and circuits.

This is especially true for disturbances coming from the I²C-bus traffic, whatever this traffic is intended for the MOPLL or for another slave on the bus.

To avoid this I²C-bus crosstalk and be able to have a clean noise spectrum, it is necessary to use a bus gate that enables the signal on the bus to drive the MOPLL only when the communication is intended for the tuner part (such a kind of I²C-bus gate is included into the Philips terrestrial channel decoders), and to avoid unnecessary repeated sending of the same information.

8 I²C-BUS PROTOCOL

The TDA6650TT; TDA6651TT is controlled via the two-wire I²C-bus. For programming, there is one device address (7 bits) and the R/$\overline{W}$ bit for selecting read or write mode. To be able to have more than one MOPLL in an I²C-bus system, one of four possible addresses is selected depending on the voltage applied to address selection pin AS (see Table 5).

The TDA6650TT; TDA6651TT fulfils the fast mode I²C-bus, according to the Philips I²C-bus specification (see Chapter 20), except for the timing as described in Fig.4. The I²C-bus interface is designed in such a way that the pins SCL and SDA can be connected to 5, 3.3 or to 2.5 V pulled-up I²C-bus lines, depending on the voltage applied to pin BVS (see Table 2).

8.1 Write mode; R/$\overline{W}$ = 0

After the address transmission (first byte), data bytes can be sent to the device (see Table 3). Five data bytes are needed to fully program the TDA6650TT; TDA6651TT. The I^{2}C-bus transceiver has an auto-increment facility that permits programming the device within one single transmission (address + 5 data bytes).

The TDA6650TT; TDA6651TT can also be partly programmed on the condition that the first data byte following the address is byte 2 (divider byte 1) or byte 4 (control byte 1). The first bit of the first data byte transmitted indicates whether byte 2 (first bit = 0) or byte 4 (first bit = 1) will follow. Until an I^{2}C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device. The fractional calculator is updated only at the end of the transmission (STOP condition). Each control byte is loaded after the 8th clock pulse of the corresponding control byte. Main divider data are valid only if no new I^{2}C-bus transmission is started (START condition) during the computation period of 50 μs.

Both DB1 and DB2 need to be sent to change the main divider ratio. If the value of the ratio selection bits R2, R1 and R0 are changed, the bytes DB1 and DB2 have to be sent in the same transmission.

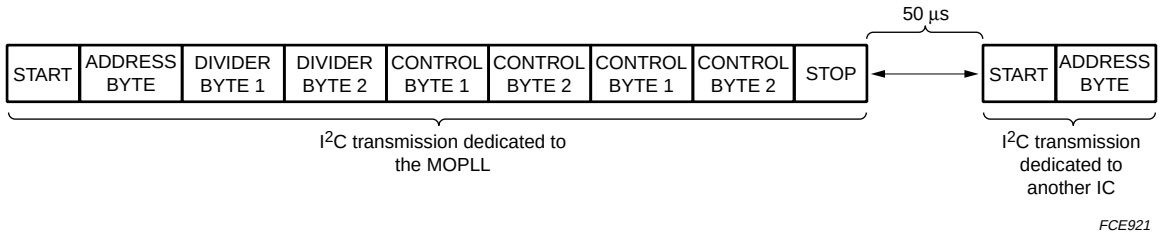


Fig.4 Example of I^{2}C-bus transmission frame.

Table 3 I^{2}C-bus write data format

NAME	BYTE	BIT								ACK
		MSB(1)							LSB	
Address byte	1	1	1	0	0	0	MA1	MA0	R/$\overline{W}$ = 0	A
Divider byte 1 (DB1)	2	0	N14	N13	N12	N11	N10	N9	N8	A
Divider byte 2 (DB2)	3	N7	N6	N5	N4	N3	N2	N1	N0	A
Control byte 1 (CB1); see Table 4	4	1	T/A = 1	T2	T1	T0	R2	R1	R0	A
		1	T/A = 0	0	0	ATC	AL2	AL1	AL0	A
Control byte 2 (CB2)	5	CP2	CP1	CP0	BS5	BS4	BS3	BS2	BS1	A

Note

1. MSB is transmitted first.

Table 4 Description of write data format bits

BIT	DESCRIPTION
A	acknowledge
MA1 and MA0	programmable address bits; see Table 5
R/$\overline{W}$	logic 0 for write mode
N14 to N0	programmable LO frequency; N = N14 $\times$ 2^{14} + N13 $\times$ 2^{13} + N12 $\times$ 2^{12} + ... + N1 $\times$ 2^{1} + N0
T/A	test/AGC bit T/A = 0: the next six bits sent are AGC settings T/A = 1: the next six bits sent are test and reference divider ratio settings
T2, T1 and T0	test bits; see Table 6
R2, R1, and R0	reference divider ratio and programmable frequency step; see Table 7
ATC	AGC current setting and time constant; capacitor on pin AGC = 150 nF ATC = 0: AGC current = 220 nA; AGC time constant = 2 s ATC = 1: AGC current = 9 μA; AGC time constant = 50 ms
AL2, AL1 and AL0	AGC take-over point bits; see Table 8
CP2, CP1 and CP0	charge pump current; see Table 9
BS5, BS4, BS3, BS2 and BS1	PMOS ports control bits BSn = 0: corresponding port is off, high-impedance state (status at Power-on reset) BSn = 1: corresponding port is on; $V_O = V_{CC} - V_{DS(sat)}$

8.1.1 I^2C-BUS ADDRESS SELECTION

The device address contains programmable address bits MA1 and MA0, which offer the possibility of having up to four MOPLL ICs in one system. Table 5 gives the relationship between the voltage applied to the AS input and the MA1 and MA0 bits.

Table 5 Address selection

VOLTAGE APPLIED TO PIN AS	MA1	MA0
0 V to 0.1V_{CC}	0	0
0.2V_{CC} to 0.3V_{CC} or open-circuit	0	1
0.4V_{CC} to 0.6V_{CC}	1	0
0.9V_{CC} to V_{CC}	1	1

8.1.2 XTOUT OUTPUT BUFFER AND MODE SETTING

The crystal frequency can be sent to pin XTOUT and used in the application, for example to drive the clock input of a digital demodulator, saving a quartz crystal in the bill of material. To output f_{xtal}, it is necessary to set T[2:0] to 001. If the output signal on this pin is not used, it is recommended to disable it, by setting T[2:0] to 000. This pin is also used to output $^1/_2 f_{div}$ and f_{comp} in a test mode. At Power-on, the XTOUT output buffer is set to on, supplying the f_{xtal} signal. The relation between the signal on pin XTOUT and the setting of theT[2:0] bits is given in Table 6.

Table 6 XTOUT buffer status and test modes

T2	T1	T0	PIN XTOUT	MODE
0	0	0	disabled	normal mode with XTOUT buffer off
0	0	1	f_{xtal} (4 MHz)	normal mode with XTOUT buffer on
0	1	0	$^1/_2 f_{div}$	charge pump off
0	1	1	f_{xtal} (4 MHz)	switch ALBC on or off (note 1)
1	0	0	f_{comp}	test mode
1	0	1	$^1/_2 f_{div}$	test mode
1	1	0	f_{xtal} (4 MHz)	charge pump sinking current (note 2)
1	1	1	disabled	charge pump sourcing current

Notes

1. Automatic Loop Bandwidth Control (ALBC) is disabled at Power-on reset. After Power-on reset this feature is enabled by setting T[2:0] = 011. To disable again the ALBC, set T[2:0] = 011 again. This test mode acts like a toggle switch, which means each time it is set the status of the ALBC changes. To toggle the ALBC, two consecutive Control byte 1s (CB1), should be sent: one byte with T[2:0] = 011 indicating that ALBC will be switched on or off and one byte programming the test mode to be selected (see Table 23, example of I^2C-bus sequence).
2. This is the default mode at Power-on reset. This mode disables the tuning voltage.

8.1.3 STEP FREQUENCY SETTING

The step frequency is set by three bits, giving five steps to cope with different application requirements.

The reference divider ratio is automatically set depending on bits R2, R1 and R0. The phase detector works at either 4, 2 or 1 MHz.

Table 7 shows the step frequencies and corresponding reference divider ratios. When the value of bits R2, R1 and R0 are changed, it is necessary to re-send the data bytes DB1 and DB2.

Table 7 Reference divider ratio select bits

R2	R1	R0	REFERENCE DIVIDER RATIO	FREQUENCY COMPARISON	FREQUENCY STEP
0	0	0	2	2 MHz	62.5 kHz
0	0	1	1	4 MHz	142.86 kHz
0	1	0	1	4 MHz	166.67 kHz
0	1	1	4	1 MHz	50 kHz
1	0	0	1	4 MHz	125 kHz
1	0	1	–	–	reserved
1	1	0	–	–	reserved
1	1	1	–	–	reserved

8.1.4 AGC DETECTOR SETTING

The AGC take-over point can be selected out of 6 levels according to Table 8.

Table 8 AGC programming

AL2	AL1	AL0	TYPICAL TAKE-OVER POINT LEVEL
0	0	0	124 dBμV (p-p)
0	0	1	121 dBμV (p-p)
0	1	0	118 dBμV (p-p)
0	1	1	115 dBμV (p-p)
1	0	0	112 dBμV (p-p)
1	0	1	109 dBμV (p-p)
1	1	0	I_{AGC} = 0; note 1
1	1	1	V_{AGC} = 3.5 V; note 2

Notes

1. The AGC current sources are disabled. The AGC output goes into a high-impedance state and an external AGC source can be connected in parallel and will not be influenced.
2. The AGC detector is disabled and I_{AGC} = 9 μA.

8.1.5 CHARGE PUMP CURRENT SETTING

The charge pump current can be chosen from 8 values depending on the value of bits CP2, CP1 and CP0 bits; see Table 9. The programming of the CP bits are not taken into account when ALBC mode is in use.

Table 9 Charge pump current

CP2	CP1	CP0	CHARGE PUMP CURRENT NUMBER	TYPICAL CURRENT (ABSOLUTE VALUE IN μA)
0	0	0	1	38
0	0	1	2	54
0	1	0	3	83
0	1	1	4	122
1	0	0	5	163
1	0	1	6	254
1	1	0	7	400
1	1	1	8	580

8.1.6 AUTOMATIC LOOP BANDWIDTH CONTROL (ALBC)

In a PLL controlled VCO in which the PLL reduces phase noise close to the carrier, there is an optimum loop bandwidth corresponding to the minimum integrated phase jitter. This loop bandwidth depends on different parameters like the VCO slope, the loop filter components, the dividing ratio and the gain of the phase detector and charge pump.

In order to reach the best phase noise performance it is necessary, especially in a wide band system like a digital tuner, to set the charge pump current to different values depending on the band and frequency used. This is to cope with the variations of the different parameters that set the bandwidth. The selection can be done in the application and requires for each frequency to program not only the divider ratios, but also the band and the best charge pump current.

The TDA6650TT; TDA6651TT includes the ALBC feature that automatically sets the band and the charge pump current, provided the IC is used in the DVB-T standard

application shown in Figs 27 and 28. This feature is activated by setting bits T[2:0] = 011 after Power-on reset. This feature is disabled when the same bits are set again. When ALBC is activated, the output ports BS1, BS2 and BS3 are not programmed by the corresponding BS bits, but are set according to Tables 10 and 11. When ALBC is active, bit ALBC = 1. Table 11 summarizes the programming of the band selection and the charge pump current when ALBC is active.

Table 10 ALBC settings

BIT				BAND SELECTED	CHARGE PUMP CURRENT	PORT		
ALBC	BS3	BS2	BS1			BS3	BS2	BS1
0	X	0	0	high	see Table 11	follows bit BS3	off	off
0	X	0	1	low			off	on
0	X	1	0	mid			on	off
0	X	1	1	forbidden				
1	X	X	X	depends on LO program, shown in Table 11				

Table 11 ALBC band selection and charge current setting

LO FREQUENCY	BAND	CHARGE PUMP CURRENT NUMBER
80 to 92 MHz	low	2
92 to 144 MHz		3
144 to 156 MHz		4
156 to 176 MHz		5
176 to 184 MHz		6
184 to 196 MHz		7
196 to 224 MHz	mid	2
224 to 296 MHz		3
296 to 380 MHz		4
380 to 404 MHz		5
404 to 448 MHz		6
448 to 472 MHz		7
472 to 484 MHz		8
484 to 604 MHz	high	4
604 to 676 MHz		5
676 to 752 MHz		6
752 to 868 MHz		7
868 to 904 MHz		8

8.2 Read mode; R/$\overline{W}$ = 1

Data can be read from the device by setting the R/$\overline{W}$ bit to 1 (see Table 12). After the device address has been recognized, the device generates an acknowledge pulse and the first data byte (status byte) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a HIGH level of the SCL clock signal.

A second data byte can be read from the device if the microcontroller generates an acknowledge on the SDA line (master acknowledge). End of transmission will occur if no master acknowledge occurs. The device will then release the data line to allow the microcontroller to generate a STOP condition.

Table 12 I^2C-bus read data format

NAME	BYTE	BIT								ACK
		MSB(1)							LSB	
Address byte	1	1	1	0	0	0	MA1	MA0	R/$\overline{W}$ = 1	A
Status byte	2	POR	FL	ALBC	1	AGC	A2	A1	A0	–

Note

1. MSB is transmitted first.

Table 13 Description of read data format bits

BIT	DESCRIPTION
A	acknowledge bit
POR	Power-on reset flag POR = 0, normal operation POR = 1, Power-on reset
FL	in-lock flag FL = 0, not locked FL = 1, the PLL is locked
ALBC	automatic loop bandwidth control flag ALBC = 0, no automatic loop bandwidth control ALBC = 1, automatic loop bandwidth control selected
AGC	internal AGC flag AGC = 0 when internal AGC is active ($V_{AGC} < V_{RML}$) AGC = 1 when internal AGC is not active ($V_{AGC} > V_{RMH}$)
A2, A1, A0	digital outputs of the 5-level ADC; see Table 14

Table 14 ADC levels

VOLTAGE APPLIED TO PIN ADC[1]	A2	A1	A0
$0.6V_{CC}$ to V_{CC}	1	0	0
$0.45V_{CC}$ to $0.6V_{CC}$	0	1	1
$0.3V_{CC}$ to $0.45V_{CC}$	0	1	0
$0.15V_{CC}$ to $0.3V_{CC}$	0	0	1
0 to $0.15V_{CC}$	0	0	0

Note

1. Accuracy is $\pm 0.03V_{CC}$. Bit BS5 must be set to logic 0 to disable the BS5 output port. The BS5 output port uses the same pin as the ADC and can not be used when the ADC is in use.

8.3 Status at Power-on reset

At power on or when the supply voltage drops below approximately 2.85 V (at T_{amb} = 25 °C), internal registers are set according to Table 15.

At power on, the charge pump current is set to 580 μA, the test bits T[2:0] are set to 110 which means that the charge pump is sinking current, the tuning voltage output is disabled and the ALBC function is disabled. The XTOUT buffer is on, driving the 4 MHz signal from the crystal oscillator and all the ports are off. As a consequence, the high band is selected by default.

Table 15 Default setting at Power-on reset

NAME	BYTE	BIT[1]							
		MSB							LSB
Address byte	1	1	1	0	0	0	MA1	MA0	X
Divider byte 1 (DB1)	2	0	N14 = X	N13 = X	N12 = X	N11 = X	N10 = X	N9 = X	N8 = X
Divider byte 2 (DB2)	3	N7 = X	N6 = X	N5 = X	N4 = X	N3 = X	N2 = X	N1 = X	N0 = X
Control byte 1 (CB1)	4	1	T/A = X; note 2	T2 = 1	T1 = 1	T0 = 0	R2 = X	R1 = X	R0 = X
		1	T/A = X; note 3	0	0	ATC = 0	AL2 = 0	AL1 = 1	AL0 = 0
Control byte 2 (CB2)	5	CP2 = 1	CP1 = 1	CP0 = 1	BS5 = 0	BS4 = 0	BS3 = 0	BS2 = 0	BS1 = 0

Notes

1. X means that this bit is not set or reset at Power-on reset.
2. The next six bits are written, when bit T/A = 1 in a write sequence.
3. The next six bits are written, when bit T/A = 0 in a write sequence.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); positive currents are entering the IC and negative currents are going out of the IC; all voltages are referenced to ground (GND); note 1

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}, V_{CCD}	supply voltage		–0.3	+6	V
V_{VT}	tuning voltage output		–0.3	+35	V
V_{SDA}	serial data input and output voltage		–0.3	+6	V
I_{SDA}	serial data output current	during acknowledge	0	10	mA
V_{SCL}	serial clock input voltage		–0.3	+6	V
V_{AS}	address selection input voltage		–0.3	+6	V
V_n	voltage on all other inputs, outputs and combined inputs and outputs, except GNDs	4.5 V< V_{CC} < 5.5 V	–0.3	V_{CC} + 0.3	V
I_{BSn}	PMOS port output current	corresponding port on; open-drain	–20	0	mA
$I_{BS(tot)}$	sum of all PMOS port output currents	open-drain	–50	0	mA
$t_{sc(max)}$	maximum short-circuit time	each pin to V_{CC} or to GND	–	10	s
T_{stg}	storage temperature		–40	+150	°C
T_{amb}	ambient temperature		–20	$T_{amb(max)}$ (2)	°C
T_j	junction temperature		–	+150	°C

Notes

1. Maximum ratings cannot be exceeded, not even momentarily without causing irreversible IC damage. Maximum ratings cannot be accumulated.
2. The maximum allowed ambient temperature $T_{amb(max)}$ depends on the assembly conditions of the package and especially on the design of the PCB. The application mounting must be done in such a way that the maximum junction temperature T_j is never exceeded. An estimation of the junction temperature can be obtained through measurement of the temperature of the top centre of the package ($T_{package}$). The temperature difference junction to case (ΔT_{j-c}) is estimated at about 13 °C on the demoboard (PCB 827-3).

   The junction temperature is: $T_j = T_{package} + \Delta T_{j-c}$

10 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

11 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	notes 1, 2 and 3		
	TDA6650TT		82	K/W
	TDA6651TT		74	K/W

Notes

1. Measured in free air as defined by JEDEC standard JESD51-2
2. These values are given for information only. The thermal resistance depends strongly on the nature and design of the PCB used in the application.The thermal resistance given corresponds to the value that can be measured on a multilayer PCB (4 layers) as defined by JEDEC standard.
3. The junction temperature influences strongly the reliability of an IC. The PCB used in the application contributes in a large part to the overall thermal characteristic. It must therefore be insured that the junction temperature of the IC never exceeds $T_{j(max)}$ = 150 °C at the maximum ambient temperature.

12 CHARACTERISTICS

V_{CCA} = V_{CCD} = 5 V, T_{amb} = 25 °C; values are given for an asymmetrical IF output loaded with a 75 Ω load or with a symmetrical IF output loaded with 1.25 kΩ; positive currents are entering the IC and negative currents are going out of the IC; the performances of the circuits are measured in the measurement circuits Figs 27 and 28 for digital application or in the measurement circuits Figs 29 and 30 for hybrid application; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	supply voltage		4.5	5.0	5.5	V
I_{CC}	supply current	PMOS ports off	80	96	115	mA
		one PMOS port on: sourcing 15 mA	96	112	131	mA
		two PMOS ports on: one port sourcing 15 mA and one other port sourcing 5 mA	101	117	136	mA
General functions						
V_{POR}	Power-on reset supply voltage	Power-on reset active if $V_{CC} < V_{POR}$	–	2.85	3.5	V
Δf_{lock}	frequency range the PLL is able to synthesize		64	–	1024	MHz
Crystal oscillator; note 1						
f_{xtal}	crystal frequency		–	4.0	–	MHz
$\lvert Z_{xtal} \rvert$	input impedance (absolute value)	f_{xtal} = 4 MHz; V_{CC} = 4.5 V to 5.5 V; T_{amb} = –20 °C to + 85 °C	350	430	–	Ω
P_{xtal}	crystal drive level	f_{xtal} = 4 MHz; note 2	–	70	–	µW
PMOS ports: pins BS1, BS2, BS3, BS4 and BS5						
$I_{LO(off)}$	output leakage current in off state	V_{CC} = 5.5 V; V_{BS} = 0 V	–10	–	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DS(sat)}$	output saturation voltage	only corresponding buffer is on, sourcing 15 mA; $V_{DS(sat)} = V_{CC} - V_{BS}$	–	0.2	0.4	V
ADC input: pin ADC						
V_i	ADC input voltage	see Table 14	0	–	5.5	V
I_{IH}	HIGH-level input current	$V_{ADC} = V_{CC}$	–	–	10	µA
I_{IL}	LOW-level input current	$V_{ADC} = 0$ V	–10	–	–	µA
Address selection input: pin AS						
I_{IH}	HIGH-level input current	$V_{AS} = 5.5$ V	–	–	10	µA
I_{IL}	LOW-level input current	$V_{AS} = 0$ V	–10	–	–	µA
Bus voltage selection input: pin BVS						
I_{IH}	HIGH-level input current	$V_{BVS} = 5.5$ V	–	–	100	µA
I_{IL}	LOW-level input current	$V_{BVS} = 0$ V	–100	–	–	µA
Buffered output: pin XTOUT						
$V_{o(p-p)}$	square wave AC output voltage (peak-to peak value)	note 3	–	400	–	mV
Z_o	output impedance		–	175	–	Ω
I²C-bus						
INPUTS: PINS SCL AND SDA						
f_{clk}	clock frequency	frequency on SCL	–	–	400	kHz
V_{IL}	LOW-level input voltage	$V_{BVS} = 0$ V	0	–	0.75	V
		$V_{BVS} = 2.5$ V or open-circuit	0	–	1.0	V
		$V_{BVS} = 5$ V	0	–	1.5	V
V_{IH}	HIGH-level input voltage	$V_{BVS} = 0$ V	1.75	–	5.5	V
		$V_{BVS} = 2.5$ V or open-circuit	2.3	–	5.5	V
		$V_{BVS} = 5$ V	3.0	–	5.5	V
I_{IH}	HIGH-level input current	$V_{CC} = 0$ V; $V_{BUS} = 5.5$ V	–	–	10	µA
		$V_{CC} = 5.5$ V; $V_{BUS} = 5.5$ V	–	–	10	µA
I_{IL}	LOW-level input current	$V_{CC} = 0$ V; $V_{BUS} = 1.5$ V	–	–	10	µA
		$V_{CC} = 5.5$ V; $V_{BUS} = 0$ V	–10	–	–	µA
OUTPUT: PIN SDA						
I_{LH}	leakage current	$V_{SDA} = 5.5$ V	–	–	10	µA
$V_{O(ack)}$	output voltage during acknowledge	$I_{SDA} = 3$ mA	–	–	0.4	V
Charge pump output: pin CP						
$\|I_o\|$	output current (absolute value)	see Table 9	–	–	–	µA
$I_{L(off)}$	off-state leakage current	charge pump off (T[2:0] = 010)	–15	0	+15	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Tuning voltage output: pin VT						
$I_{L(off)}$	leakage current when switched-off	tuning supply voltage = 33 V	–	–	10	μA
$V_{o(cl)}$	output voltage when the loop is closed	charge pump off (T[2:0] = 010); tuning supply voltage = 33 V; R_L = 15 kΩ	0.3	–	32.7	V
Noise performance						
$J_{\phi(rms)}$	phase jitter (RMS value)	integrated between 1 kHz and 1 MHz offset from the carrier				
		digital application	–	0.5	–	deg
		hybrid application	–	0.6	–	deg
Low band mixer, including IF amplifier						
f_{RF}	RF frequency	picture carrier; note 4	43.25	–	157.25	MHz
G_v	voltage gain	asymmetrical IF output; R_L = 75 Ω; see Fig.14				
		f_{RF} = 44.25 MHz	21	24	27	dB
		f_{RF} = 157.25 MHz	21	24	27	dB
		symmetrical IF output; R_L = 1.25 kΩ; see Fig.15				
		f_{RF} = 44.25 MHz	25	28	31	dB
		f_{RF} = 157.25 MHz	25	28	31	dB
NF	noise figure	see Figs 16 and 17				
		f_{RF} = 50 MHz	–	8.0	10.0	dB
		f_{RF} = 150 MHz	–	8.0	10.0	dB
V_o	output voltage causing 1% cross modulation in channel	asymmetrical application; see Fig.18; note 5				
		f_{RF} = 44.25 MHz	107	110	–	dBμV
		f_{RF} = 157.25 MHz	107	110	–	dBμV
		symmetrical application; see Fig.19; note 5				
		f_{RF} = 44.25 MHz	117	120	–	dBμV
		f_{RF} = 157.25 MHz	117	120	–	dBμV
V_i	input voltage causing 750 Hz frequency deviation pulling in channel	asymmetrical IF output	–	90	–	dBμV
INT_{SO2}	channel SO2 beat	V_{RFpix} = 80 dBμV; note 6	57	60	–	dBc
$V_{i(lock)}$	input level without lock-out	see Fig.25; note 7	–	–	120	dBμV
G_i	input conductance	f_{RF} = 44.25 MHz; see Fig.5	–	0.13	–	mS
		f_{RF} = 157.25 MHz; see Fig.5	–	0.11	–	mS
C_i	input capacitance	f_{RF} = 44.25 to 157.25 MHz; see Fig.5	–	1.36	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Mid band mixer, including IF amplifier						
f_{RF}	RF frequency	picture carrier; note 4	157.25	–	443.25	MHz
G_v	voltage gain	asymmetrical IF output; load = 75 Ω; see Fig.14				
		f_{RF} = 157.25 MHz	21	24	27	dB
		f_{RF} = 443.25 MHz	21	24	27	dB
		symmetrical IF output; load = 1.25 kΩ; see Fig.15				
		f_{RF} = 157.25 MHz	25	28	31	dB
		f_{RF} = 443.25 MHz	25	28	31	dB
NF	noise figure	see Figs 16 and 17				
		f_{RF} = 150 MHz	–	8.0	10.0	dB
		f_{RF} = 300 MHz	–	9.0	11.0	dB
V_o	output voltage causing 1% cross modulation in channel	asymmetrical application; see Fig.18; note 5				
		f_{RF} = 157.25 MHz	107	110	–	dBμV
		f_{RF} = 443.25 MHz	107	110	–	dBμV
		symmetrical application; see Fig.19; note 5				
		f_{RF} = 157.25 MHz	117	120	–	dBμV
		f_{RF} = 443.25 MHz	117	120	–	dBμV
$V_{f(N+5)-1}$	(N + 5) – 1 MHz pulling	$f_{RF(wanted)}$ = 443.25 MHz; f_{osc} = 482.15 MHz; $f_{RF(unwanted)}$ = 482.25 MHz; note 8	–	80	–	dBμV
V_i	input voltage causing 750 Hz frequency deviation pulling in channel	asymmetrical IF output	–	89	–	dBμV
$V_{i(lock)}$	input level without lock-out	see Fig.25; note 7	–	–	120	dBμV
G_i	input conductance	see Fig.6	–	0.3	–	mS
C_i	input capacitance	see Fig.6	–	1.1	–	pF
High band mixer, including IF amplifier						
f_{RF}	RF frequency	picture carrier; note 4	443.25	–	863.25	MHz
G_v	voltage gain	asymmetrical IF output; load = 75 Ω; see Fig.20				
		f_{RF} = 443.25 MHz	31.5	34.5	37.5	dB
		f_{RF} = 863.25 MHz	31.5	34.5	37.5	dB
		symmetrical IF output; load = 1.25 kΩ; see Fig.21				
		f_{RF} = 443.25 MHz	35.5	38.5	41.5	dB
		f_{RF} = 863.25 MHz	35.5	38.5	41.5	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
NF	noise figure, not corrected for image	see Fig.22				
		f_{RF} = 443.25 MHz	–	6.0	8.0	dB
		f_{RF} = 863.25 MHz	–	7.0	9.0	dB
V_o	output voltage causing 1% cross modulation in channel	asymmetrical application; see Fig.23; note 5				
		f_{RF} = 443.25 MHz	107	110	–	dBμV
		f_{RF} = 863.25 MHz	107	110	–	dBμV
		symmetrical application; see Fig.24; note 5				
		f_{RF} = 443.25 MHz	117	120	–	dBμV
		f_{RF} = 863.25 MHz	117	120	–	dBμV
$V_{i(lock)}$	input level without lock-out	see Fig.26; note 7	–	–	120	dBμV
$V_{f(N+5)-1}$	(N + 5) – 1 MHz pulling	$f_{RF(wanted)}$ = 815.25 MHz; f_{osc} = 854.15 MHz; $f_{RF(unwanted)}$ = 854.25 MHz; note 8	–	80	–	dBμV
V_i	input voltage causing 750 Hz frequency deviation pulling in channel	asymmetrical IF output	–	79	–	dBμV
Z_i	input impedance ($R_S + jL_S\omega$)	f_{RF} = 443.25 MHz; see Fig.7				
		R_S	–	35	–	Ω
		L_S	–	8	–	nH
		f_{RF} = 863.25 MHz; see Fig.7				
		R_S	–	36	–	Ω
		L_S	–	8	–	nH
Low band oscillator						
f_{osc}	oscillator frequency	note 9	83.15	–	196.15	MHz
$\Delta f_{osc(V)}$	oscillator frequency shift with supply voltage	note 10	–	110	–	kHz
$\Delta f_{osc(T)}$	oscillator frequency drift with temperature	ΔT = 25 °C; V_{CC} = 5 V with compensation; note 11	–	900	–	kHz
$\Phi_{osc(dig)}$	phase noise, carrier to sideband noise in digital application	±1 kHz frequency offset; f_{comp} = 4 MHz; see Figs 8, 27 and 28	82	95	–	dBc/Hz
		±10 kHz frequency offset; worst case in the frequency range; see Figs 9, 27 and 28	87	100	–	dBc/Hz
		±100 kHz frequency offset; worst case in the frequency range; see Figs 10, 27 and 28	104	110	–	dBc/Hz
		±1.4 MHz frequency offset; worst case in the frequency range; see Figs 27 and 28	–	117	–	dBc/Hz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\Phi_{osc(hyb)}$	phase noise, carrier to sideband noise in hybrid application	±1 kHz frequency offset; f_{comp} = 4 MHz; see Figs 11, 29, and 30	80	95	–	dBc/Hz
		±10 kHz frequency offset; worst case in the frequency range; see Figs 12, 29, and 30	85	96	–	dBc/Hz
		±100 kHz frequency offset; worst case in the frequency range; see Figs 13, 29, and 30	104	110	–	dBc/Hz
		±1.4 MHz frequency offset; worst case in the frequency range; see Figs 29 and 30	–	117	–	dBc/Hz
RSC_{p-p}	ripple susceptibility of V_{CC} (peak-to-peak value)	V_{CC} = 5 V ±5%; worst case in the frequency range; ripple frequency 500 kHz; note 12	15	200	–	mV
Mid band oscillator						
f_{osc}	oscillator frequency	note 9	196.15	–	482.15	MHz
$\Delta f_{osc(V)}$	oscillator frequency shift with supply voltage	note 10	–	110	–	kHz
$\Delta f_{osc(T)}$	oscillator frequency drift with temperature	ΔT = 25 °C; V_{CC} = 5 V with compensation; note 11	–	1500	–	kHz
$\Phi_{osc(dig)}$	phase noise, carrier to sideband noise in digital application	±1 kHz frequency offset; f_{comp} = 4 MHz; see Figs 8, 27 and 28	85	90	–	dBc/Hz
		±10 kHz frequency offset; worst case in the frequency range; see Figs 9, 27 and 28	87	95	–	dBc/Hz
		±100 kHz frequency offset; worst case in the frequency range; see Figs 10, 27 and 28	104	110	–	dBc/Hz
		±1.4 MHz frequency offset; worst case in the frequency range; see Figs 27 and 28	–	115	–	dBc/Hz
$\Phi_{osc(hyb)}$	phase noise, carrier to sideband noise in hybrid application	±1 kHz frequency offset; f_{comp} = 4 MHz; see Figs 11, 29 and 30	82	88	–	dBc/Hz
		±10 kHz frequency offset; worst case in the frequency range; see Figs 12, 29 and 30	85	90	–	dBc/Hz
		±100 kHz frequency offset; worst case in the frequency range; see Figs 13, 29 and 30	104	110	–	dBc/Hz
		±1.4 MHz frequency offset; worst case in the frequency range; see Figs 29 and 30	–	115	–	dBc/Hz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RSC_{p-p}	ripple susceptibility of V_{CC} (peak-to-peak value)	V_{CC} = 5 V ±5%; worst case in the frequency range; ripple frequency 500 kHz; note 12	15	140	–	mV
High band oscillator						
f_{osc}	oscillator frequency	note 9	482.15	–	902.15	MHz
$\Delta f_{osc(V)}$	oscillator frequency shift with supply voltage	note 10	–	300	–	kHz
$\Delta f_{osc(T)}$	oscillator frequency drift with temperature	ΔT = 25 °C; V_{CC} = 5 V; with compensation; note 11	–	1100	–	kHz
$\Phi_{osc(dig)}$	phase noise, carrier to sideband noise in digital application	±1 kHz frequency offset; f_{comp} = 4 MHz; see Figs 8, 27 and 28	85	89	–	dBc/Hz
		±10 kHz frequency offset; worst case in the frequency range; see Figs 9, 27 and 28	87	93	–	dBc/Hz
		±100 kHz frequency offset; worst case in the frequency range; see Figs 11, 27 and 28	104	107	–	dBc/Hz
		±1.4 MHz frequency offset; worst case in the frequency range; see Figs 27 and 28	–	117	–	dBc/Hz
$\Phi_{osc(hyb)}$	phase noise, carrier to sideband noise in hybrid application	±1 kHz frequency offset; f_{comp} = 4 MHz; see Figs 11, 29 and 30	80	85	–	dBc/Hz
		±10 kHz frequency offset; worst case in the frequency range; see Figs 12, 29 and 30	82	86	–	dBc/Hz
		±100 kHz frequency offset; worst case in the frequency range; see Figs 13, 29 and 30	104	107	–	dBc/Hz
		±1.4 MHz frequency offset; worst case in the frequency range; see Figs 29 and 30	–	117	–	dBc/Hz
RSC_{p-p}	ripple susceptibility of V_{CC} (peak-to-peak value)	V_{CC} = 5 V ±5%; worst case in the frequency range; ripple frequency 500 kHz; note 12	15	40	–	mV
IF amplifier						
Z_o	output impedance	asymmetrical IF output				
		R_S at 38.9 MHz	–	50	–	Ω
		L_S at 38.9 MHz	–	5.4	–	nH
		symmetrical IF output				
		R_S at 38.9 MHz	–	100	–	Ω
		L_S at 38.9 MHz	–	10.4	–	nH

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Rejection at the IF output (IF amplifier in asymmetrical mode)						
INT_{div}	divider interferences in IF level	worst case; note 13	–	–	20	dBμV
INT_{xtal}	crystal oscillator interferences rejection	V_{IF} = 100 dBμV; worst case in the frequency range; note 14	–	–	–50	dBc
$INT_{f(step)}$	step frequency rejection	measured in digital application for DVB-T; f_{step} = 166.67 kHz; IF = 36.125 MHz; note 15	–	–	–50	dBc
		measured in hybrid application for DVB-T; f_{step} = 166.67 kHz; IF = 36.125 MHz; note 15	–	–	–57	dBc
		measured in hybrid application for PAL; f_{step} = 62.5 kHz; IF = 38.9 MHz; note 15	–	–	–57	dBc
		measured in hybrid application for FM; f_{step} = 50 kHz; IF = 38.9 MHz; note 15	–	–	–57	dBc
INT_{XTH}	crystal oscillator harmonics in the IF frequency	note 16	–	–	45	dBμV
AGC output (IF amplifier in asymmetrical mode): pin AGC						
$AGC_{TOP(p-p)}$	AGC take-over point (peak-to-peak level)	bits AL[2:0] = 000	122.5	124	125.5	dBμV
$I_{source(fast)}$	source current fast		7.5	9.0	11.6	μA
$I_{source(slow)}$	source current slow		185	220	280	nA
V_o	output voltage	maximum level	3.45	3.55	3.8	V
		minimum level	0	–	0.1	V
$V_{o(dis)}$	output voltage with AGC disabled	bits AL[2:0] = 111	3.45	3.55	3.8	V
$V_{RF(slip)}$	RF voltage range to switch the AGC from active to not active mode		–	–	0.5	dB
V_{RML}	low threshold AGC output voltage	AGC bit = 0 or AGC not active	0	–	2.8	V
V_{RMH}	high threshold AGC output voltage	AGC bit = 1 or AGC active	3.2	3.55	3.8	V
I_{LO}	leakage current	bits AL[2:0] = 110; $0 < V_{AGC} < V_{CC}$	–50	–	+50	nA

Notes

1. Important recommendation: to obtain the performances mentioned in this specification, the serial resistance of the crystal used with this oscillator must never exceed 120 Ω. The crystal oscillator is guaranteed to operate for any supply voltage between 4.5 V and 5.5 V and at any temperature between –20 °C and +85 °C
2. The drive level is expected with a 50 Ω series resistance of the crystal at series resonance. The drive level will be different with other series resistance values.
3. The V_{XTOUT} level is measured when the pin XTOUT is loaded with 5 kΩ in parallel with 10 pF.
4. The RF frequency range is defined by the oscillator frequency range and the intermediate frequency (IF).
5. The 1% cross modulation performance is measured with AGC detector turned off (AGC bits set to 110).
6. Channel SO2 beat is the interfering product of f_{RFpix}, f_{IF} and f_{osc} of channel SO2; f_{beat} = 37.35 MHz. The possible mechanisms are: $f_{osc} - 2 \times f_{IFpix}$ or $2 \times f_{RFpix} - f_{osc}$.
7. The IF output signal stays stable within the range of the step frequency for any RF input level up to 120 dBμV.
8. (N + 5) – 1 MHz pulling is the input level of channel N + 5, at frequency 1 MHz lower, causing 100 kHz FM sidebands 30 dB below the wanted carrier.
9. Limits are related to the tank circuits used in Figs 27 and 28 for digital application or Figs 29 and 30 for hybrid application. Frequency bands may be adjusted by the choice of external components.
10. The frequency shift is defined as a change in oscillator frequency when the supply voltage varies from V_{CC} = 5 to 4.5 V or from V_{CC} = 5 to 5.25 V. The oscillator is free running during this measurement.
11. The frequency drift is defined as a change in oscillator frequency when the ambient temperature varies from T_{amb} = 25 to 50 °C or from T_{amb} = 25 to 0 °C. The oscillator is free running during this measurement.
12. The supply ripple susceptibility is measured in the measurement circuit according to Figs 27, 28, 29 and 30 using a spectrum analyser connected to the IF output. An unmodulated RF signal is applied to the test board RF input. A sinewave signal with a frequency of 500 kHz is superimposed onto the supply voltage. The amplitude of this ripple signal is adjusted to bring the 500 kHz sidebands around the IF carrier to a level of –53.5 dB with respect to the carrier.
13. This is the level of divider interferences close to the IF frequency. For example channel S3: f_{osc} = 158.15 MHz, $\frac{1}{4} f_{osc}$ = 39.5375 MHz. The low and mid band inputs must be left open (i.e. not connected to any load or cable); the high band inputs are connected to an hybrid.
14. Crystal oscillator interference means the 4 MHz sidebands caused by the crystal oscillator.
15. The step frequency rejection is the level of step frequency sidebands (e.g. 166.67 kHz) related to the carrier.
16. This is the level of the 9th and 11th harmonics of the 4 MHz crystal oscillator into the IF output.

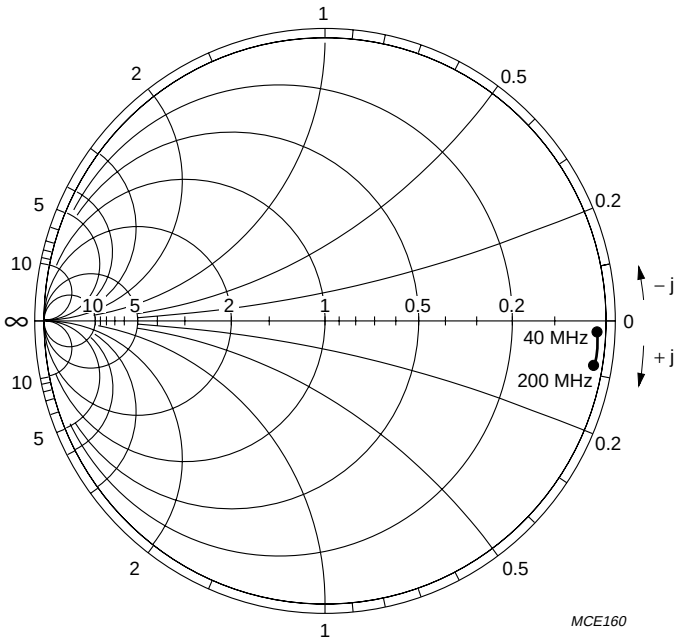


Fig.5 Input admittance (S_{11}) of the low band mixer (40 to 200 MHz); Y_o = 20 mS.

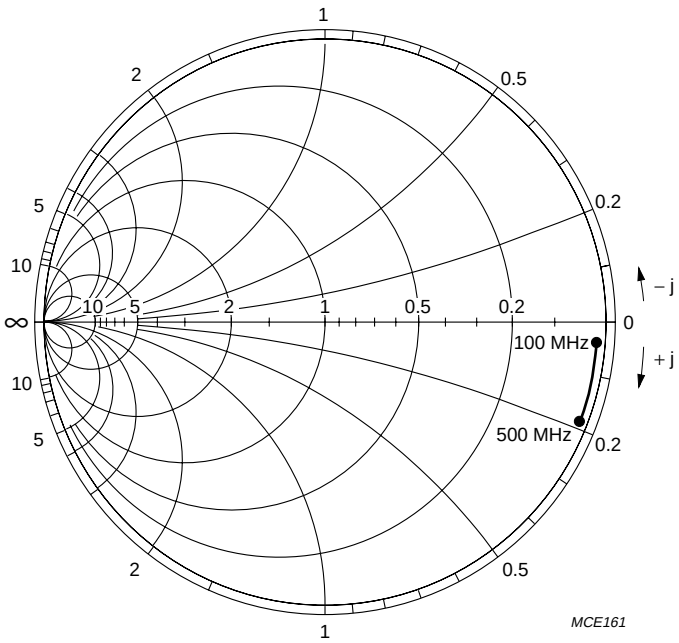


Fig.6 Input admittance (S_{11}) of the mid band mixer (100 to 500 MHz); Y_o = 20 mS.

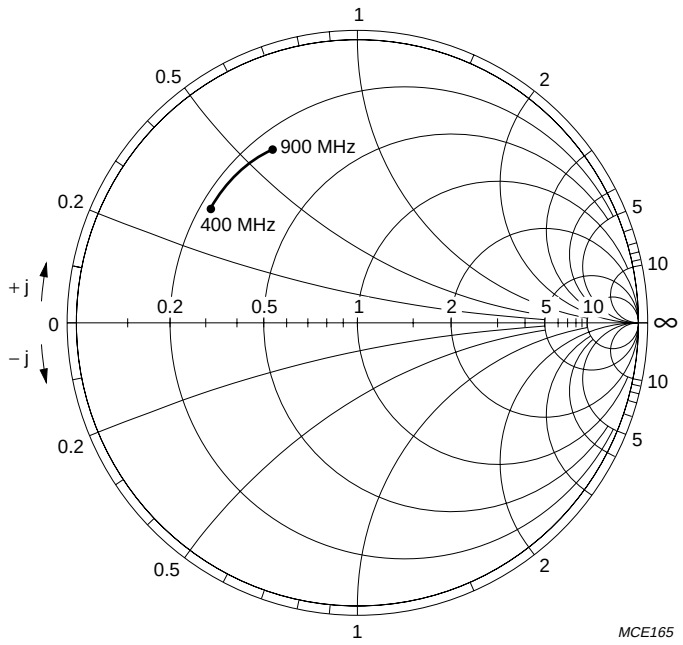


Fig.7 Input impedance (S_{11}) of the high band mixer (400 to 900 MHz); Z_o = 100 Ω.

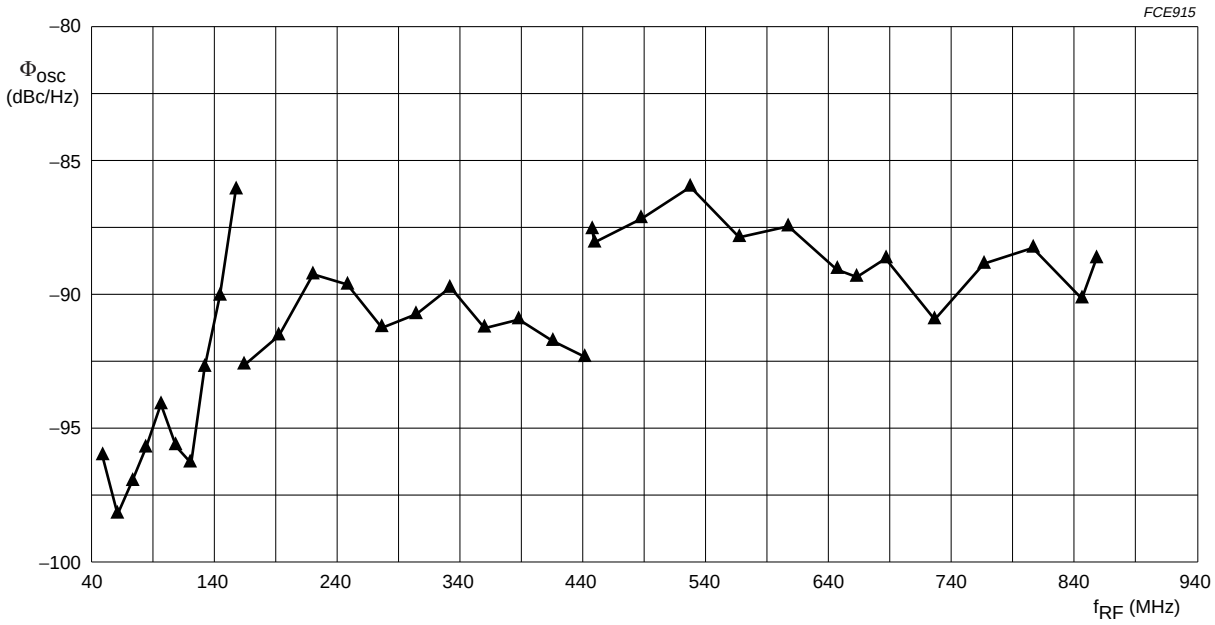


Fig.8 1 kHz phase noise typical performance in digital application (Figs 27 and 28).

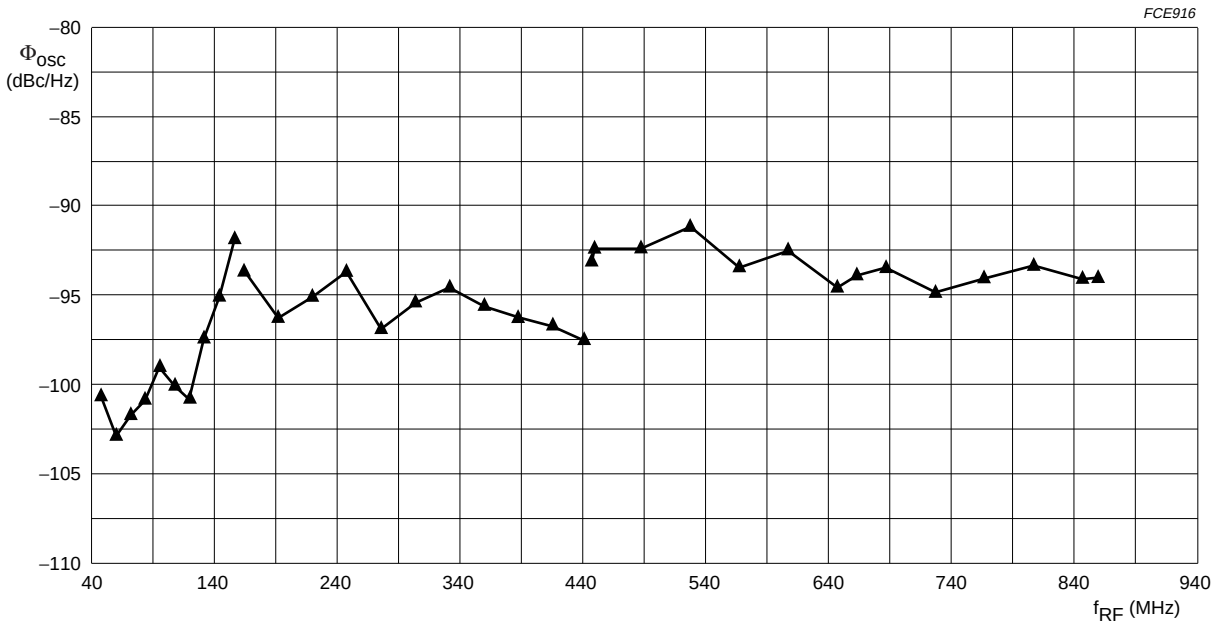


Fig.9 10 kHz phase noise typical performance in digital application (Figs 27 and 28).

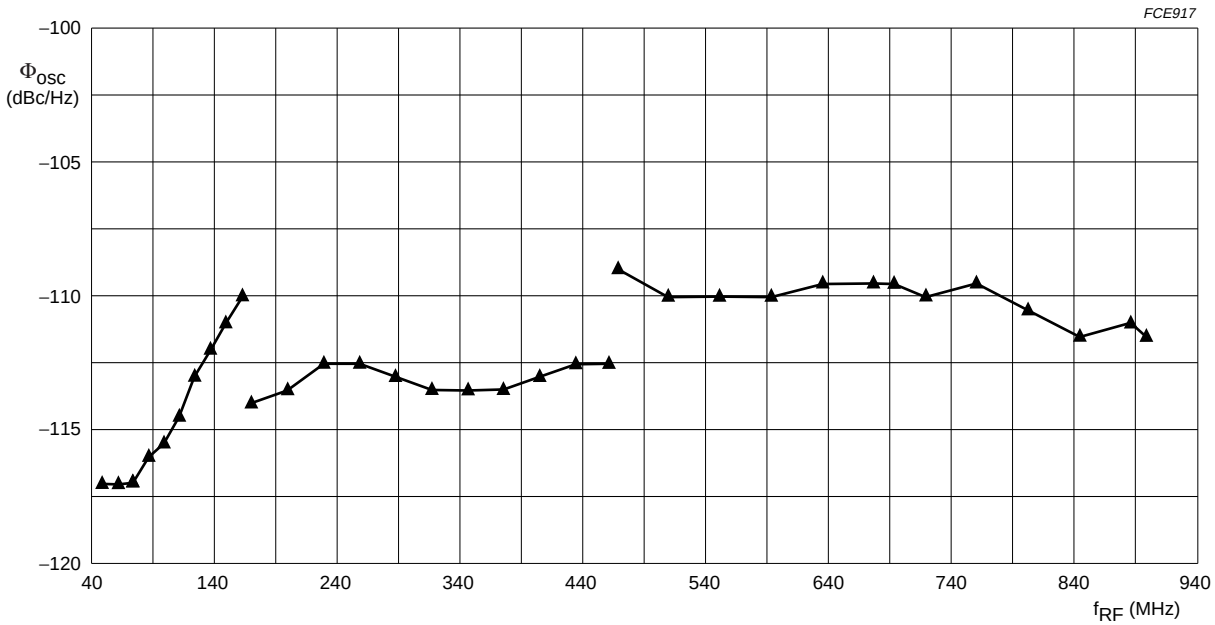


Fig.10 100 kHz phase noise typical performance in digital application (Figs 27 and 28).

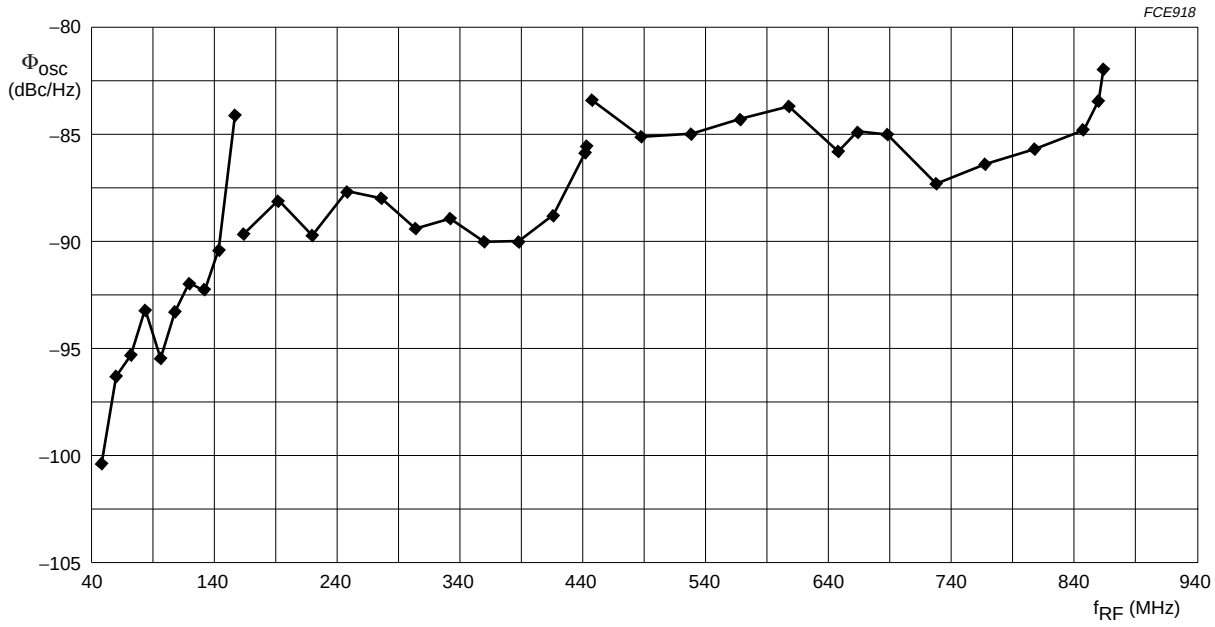


Fig.11 1 kHz phase noise typical performance in hybrid application (Figs 29 and 30).

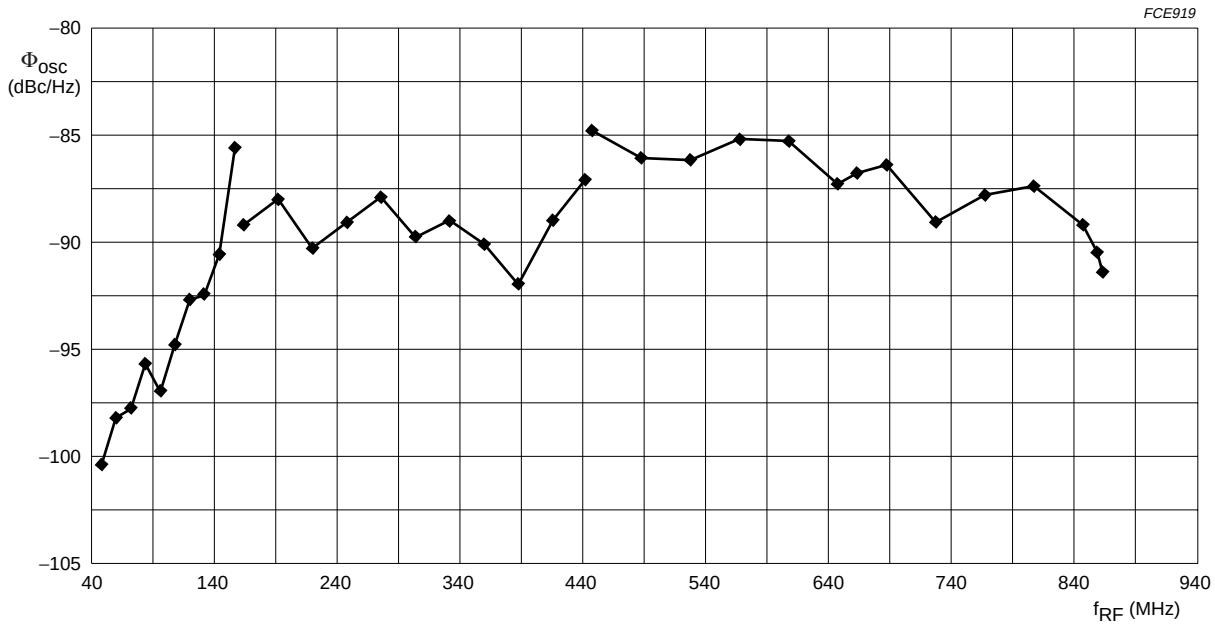


Fig.12 10 kHz phase noise typical performance in hybrid application (Figs 29 and 30).

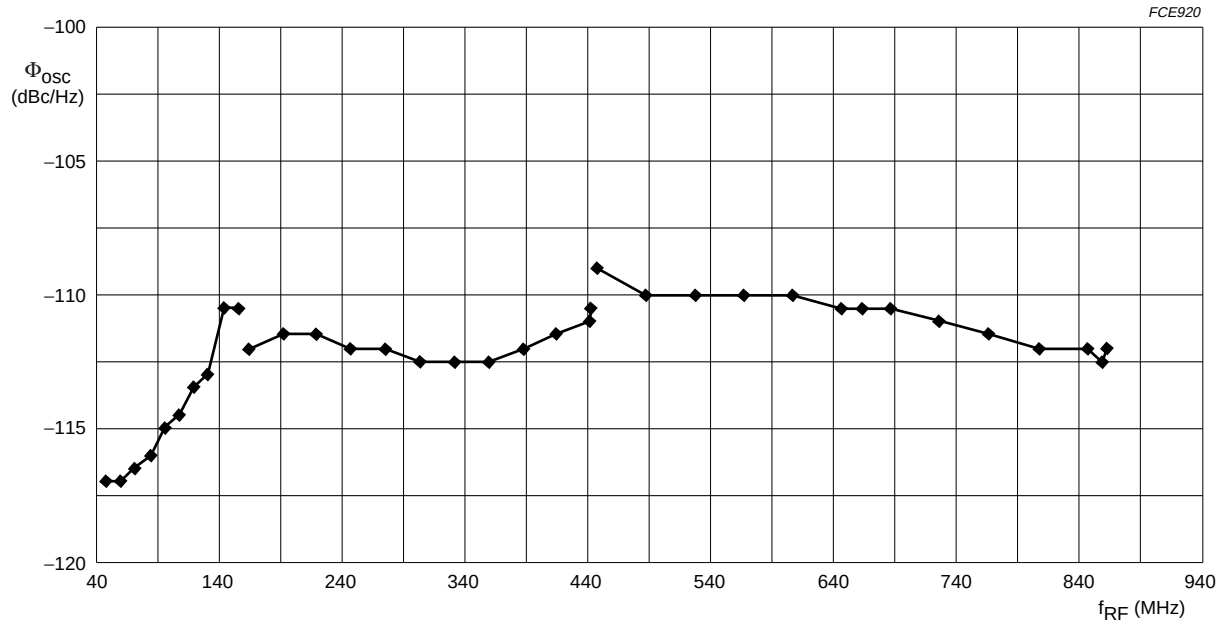
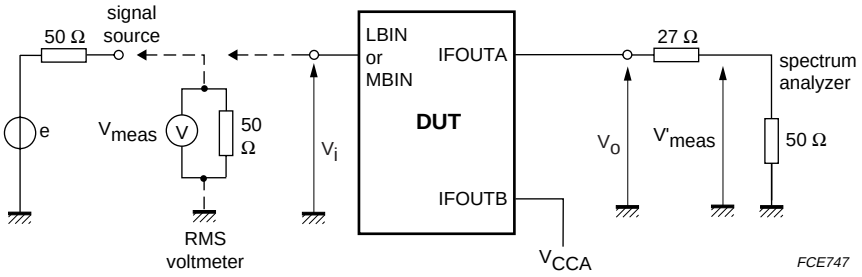


Fig.13 100 kHz phase noise typical performance in hybrid application (Figs 29 and 30).

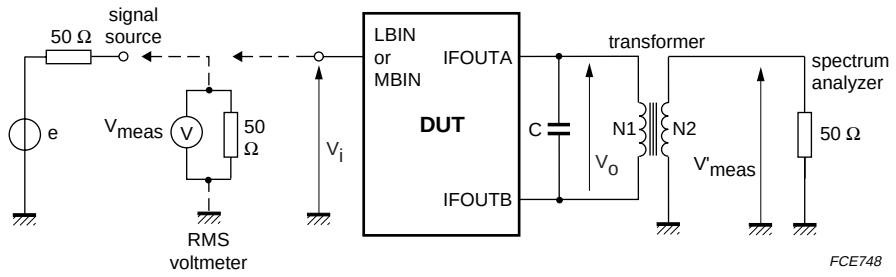


$Z_i >> 50\ \Omega \rightarrow V_i = 2 \times V_{meas} = 70\ dB\mu V$.
$V_i = V_{meas} + 6\ dB = 70\ dB\mu V$.
$V_o = V'_{meas} + 3.75\ dB$.

$G_v = 20 \log \frac{V_o}{V_i}$.

DVB-T and PAL.
IF = 38.9 MHz.

Fig.14 Gain (G_V) measurement in low and mid band with asymmetrical IF output.



$Z_i >> 50\ \Omega \rightarrow V_i = 2 \times V_{meas} = 70\ dB\mu V$.

$V_i = V_{meas} + 6\ dB = 70\ dB\mu V$.

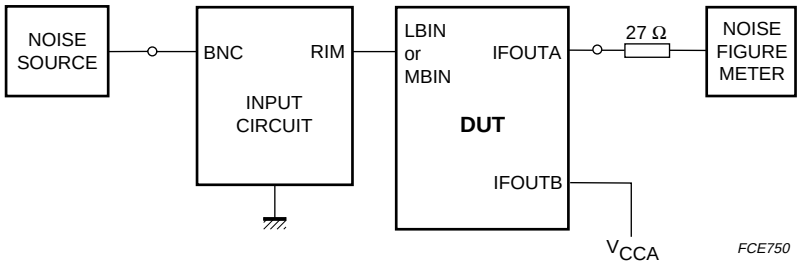
$V_o = V'_{meas} + 15\ dB$ (transformer ratio N2/N1 = 5 and transformer loss).

$G_v = 20 \log \frac{V_o}{V_i}$.

N1 = 10 turns.
N2 = 2 turns.
N1/N2 = 5.

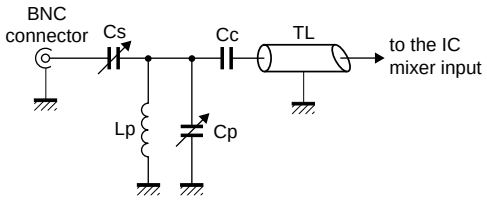
DVB-T and PAL.
IF = 38.9 MHz.

Fig.15 Gain (G_V) measurement in low and mid band with symmetrical IF output.

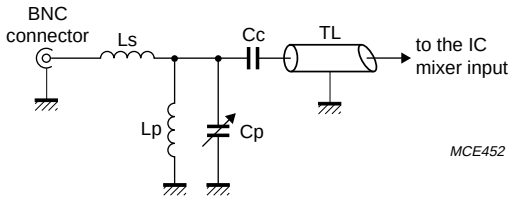


$NF = NF_{meas}$ – loss of input circuit (dB).

Fig.16 Noise figure (NF) measurement in low and mid band with asymmetrical IF output.



Schematic A.



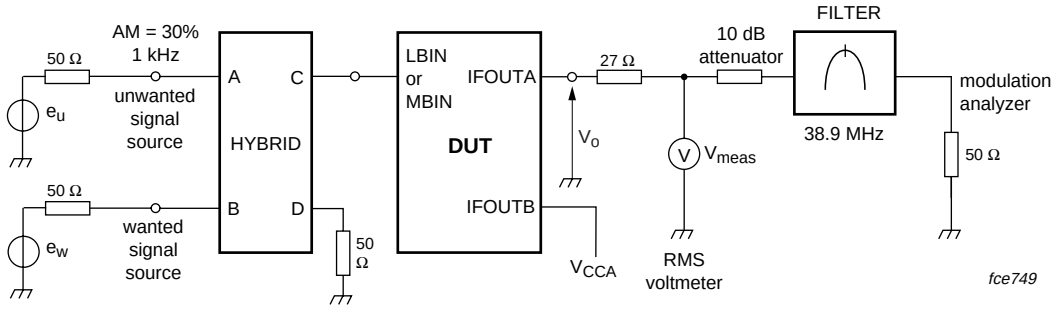
Schematic B.

For f_{RF} = 50 MHz (Schematic A)
Loss = 0 dB.
Cs = 12 pF in parallel with a 0.8 pF to 8 pF trimmer.
Cp = 18 pF in parallel with a 0.8 pF to 8 pF trimmer.
Cc = 4.7 nF.
Lp = 8 turns, ∅ 5 mm, wire ∅ = 0.4 mm air coil
TL = 50 Ω semi rigid cable, length = 75 mm.

For f_{RF} = 150 MHz (Schematic A)
Loss = 0 dB.
Cs = 0.8 pF to 8 pF trimmer.
Cp = 0.4 pF to 2.5 pF trimmer.
Cc = 4.7 nF.
Lp = 4 turns, ∅ 4.5 mm, wire ∅ = 0.4 mm air coil
TL = 50 Ω semi rigid cable, length = 75 mm.

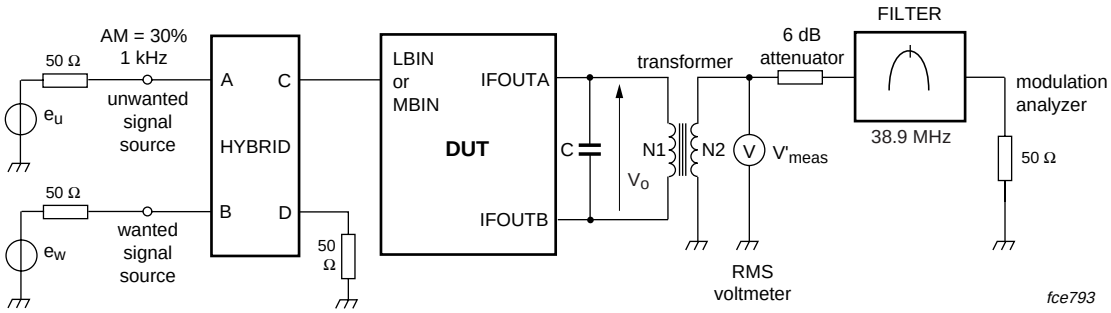
For f_{RF} = 300 MHz (Schematic B)
Loss = 0.5 dB.
Cp = 8.2 pF in parallel with a 0.8 pF to 8 pF trimmer.
Cc = 4.7 nF.
Ls = 2 turns, ∅ 1.5 mm, wire ∅ = 0.4 mm air coil.
Lp = 2 turns, ∅ 1.5 mm, wire ∅ = 0.4 mm air coil.
TL = 50 Ω semi rigid cable, length = 75 mm.

Fig.17 Input circuit for optimum noise figure in low and mid band.



$V_o = V_{meas}$ + 3.75 dB.
Wanted signal source at f_{RFpix} is 80 dBµV.
Unwanted output signal at f_{snd}.
The level of unwanted signal is measured by causing 1% AM modulation in the wanted signal.

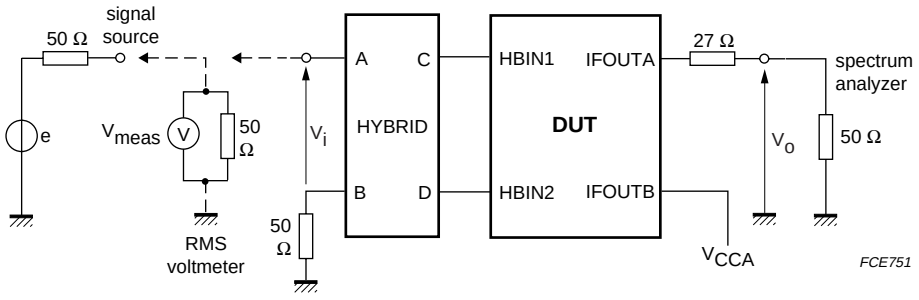
Fig.18 Cross modulation measurement in low and mid band with asymmetrical IF output.



$V'_{meas} = V_o$ – (transformer ratio N1/N2 = 5 and loss).
Wanted signal source at f_{RFpix} is 80 dBµV.
The level of unwanted signal V_o at f_{snd} is measured by causing 1% AM modulation in the wanted output signal.

N1 = 10 turns.
N2 = 2 turns.
N1/N2 = 5.

Fig.19 Cross modulation measurement in low and mid band with symmetrical IF output.

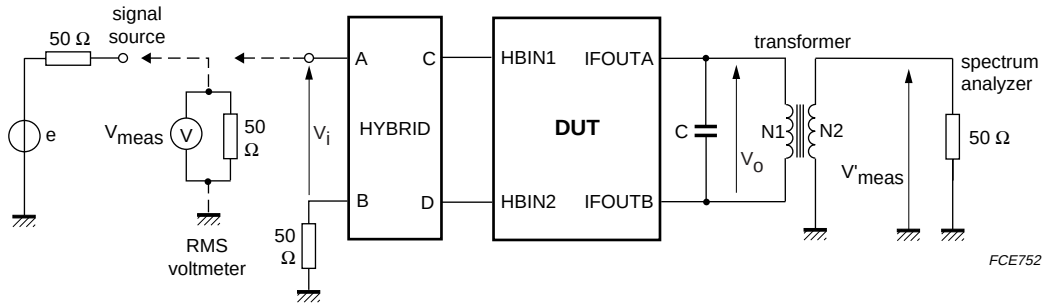


Loss in hybrid = 1 dB.
$V_i = V_{meas}$ – loss = 70 dBµV.
$V_o = V'_{meas}$ + 3.75 dB.

$G_v = 20 \log \frac{V_o}{V_i}$.

DVB-T and PAL.
IF = 38.9 MHz.

Fig.20 Gain (G_{Va}) measurement in high band with asymmetrical IF output.



Loss in hybrid = 1 dB.

$V_i = V_{meas}$ – loss = 70 dBµV.

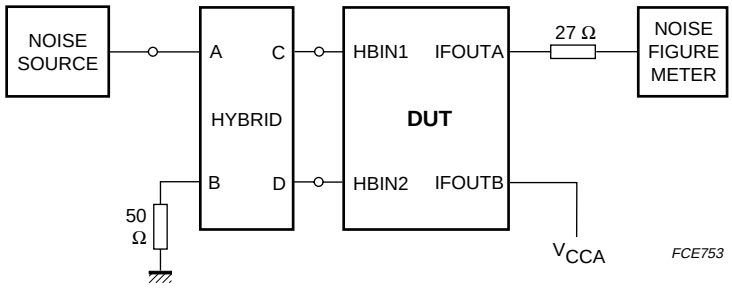
$V_o = V'_{meas}$ + 15 dB (transformer ratio N2/N1 = 5 and transformer loss).

$G_v = 20 \log \frac{V_o}{V_i}$.

DVB-T and PAL.

IF = 38.9 MHz.

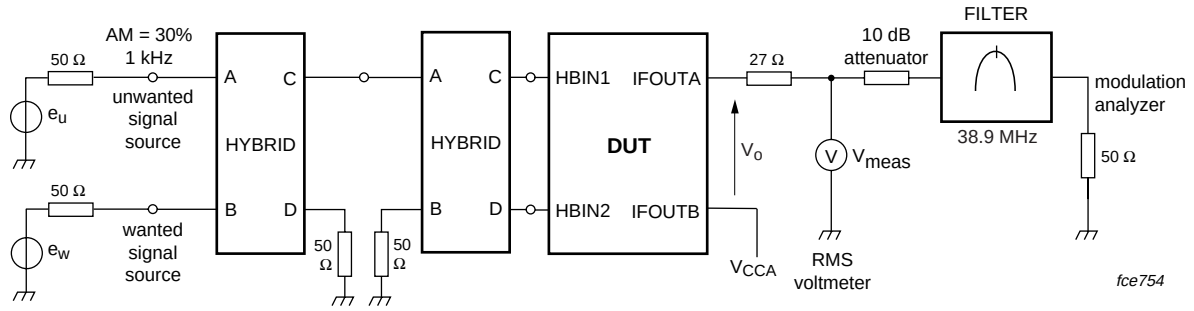
Fig.21 Gain (G_{VS}) measurement in high band with symmetrical IF output.



Loss in hybrid = 1 dB.

$NF = NF_{meas}$ – loss.

Fig.22 Noise figure (NF) measurement in high band with asymmetrical IF output.

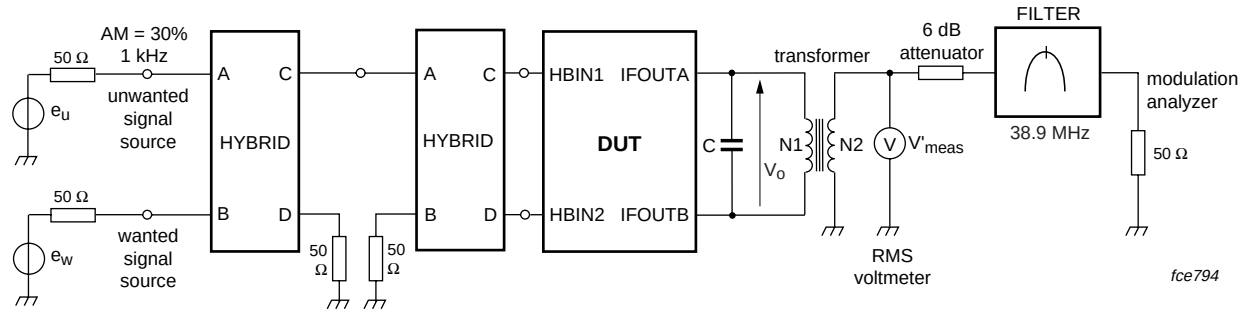


Wanted signal source at f_{RFpix} is 70 dBµV.

Unwanted output signal at f_{snd}.

The level of unwanted signal is measured by causing 1% AM modulation in the wanted signal.

Fig.23 Cross modulation measurement in high band with asymmetrical IF output.



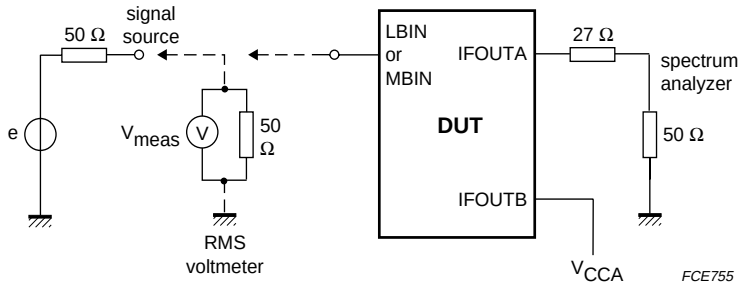
$V'_{meas} = V_o$ – (transformer ratio N1/N2 = 5 and loss).

N1 = 10 turns.

N2 = 2 turns.

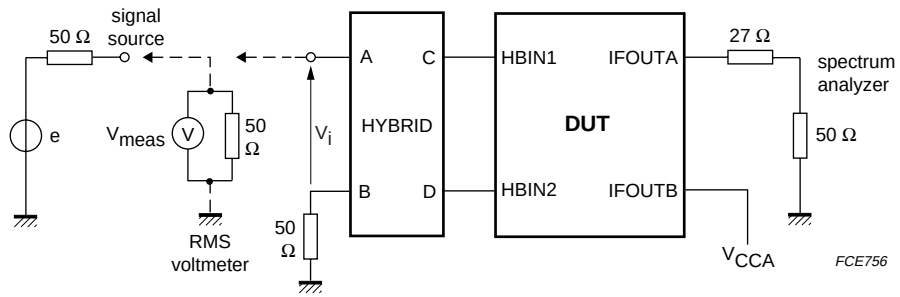
N1 / N2 = 5.

Fig.24 Cross modulation measurement in high band with symmetrical IF output.



$Z_i >> 50\ \Omega \rightarrow V_i = 2 \times V_{meas}$.
$V_i = V_{meas} + 6$ dB.

Fig.25 Maximum RF input level without lock-out in low and mid band with asymmetrical IF output.



Loss in hybrid = 1 dB.
$V_i = V_{meas}$ – loss.

Fig.26 Maximum RF input level without lock-out in high band with asymmetrical IF output.

The TDA6650TT, TDA6651TT PLL loop stability is guaranteed in the configuration of Figs. 27, 28, 29 and 30. In this configuration, the external supply source is 30 V minimum, the pull-up resistor R19, is 15 kΩ and all of the local oscillators are aligned to operate at a maximum tuning voltage of 26 V. If the configuration is changed, there might be an impact on the loop stability.

For any other configurations, a stability analysis must be performed. The conventional PLL AC model (cf. SIMPATA Philips software) used for the stability analysis, is valid provided the external source (DC supply source or DC-to-DC converter) is able to deliver a minimum current that is equal to the charge pump current in use.

The delivered current can be simply calculated with the following formula:

$$I_{delivered} = \left(\frac{V_{DC} - V_T}{R_{pu}}\right) > I_{CP}$$

Where

$I_{delivered}$ is the delivered current

V_{DC} is the supply source voltage or DC-to-DC converter output voltage

V_T is the tuning voltage

R_{pu} is the pull-up resistor between the DC supply source (or the DC-to-DC converter output) and the tuning line (R19 in Figs. 27 to 30)

I_{CP} is the charge pump current in use.

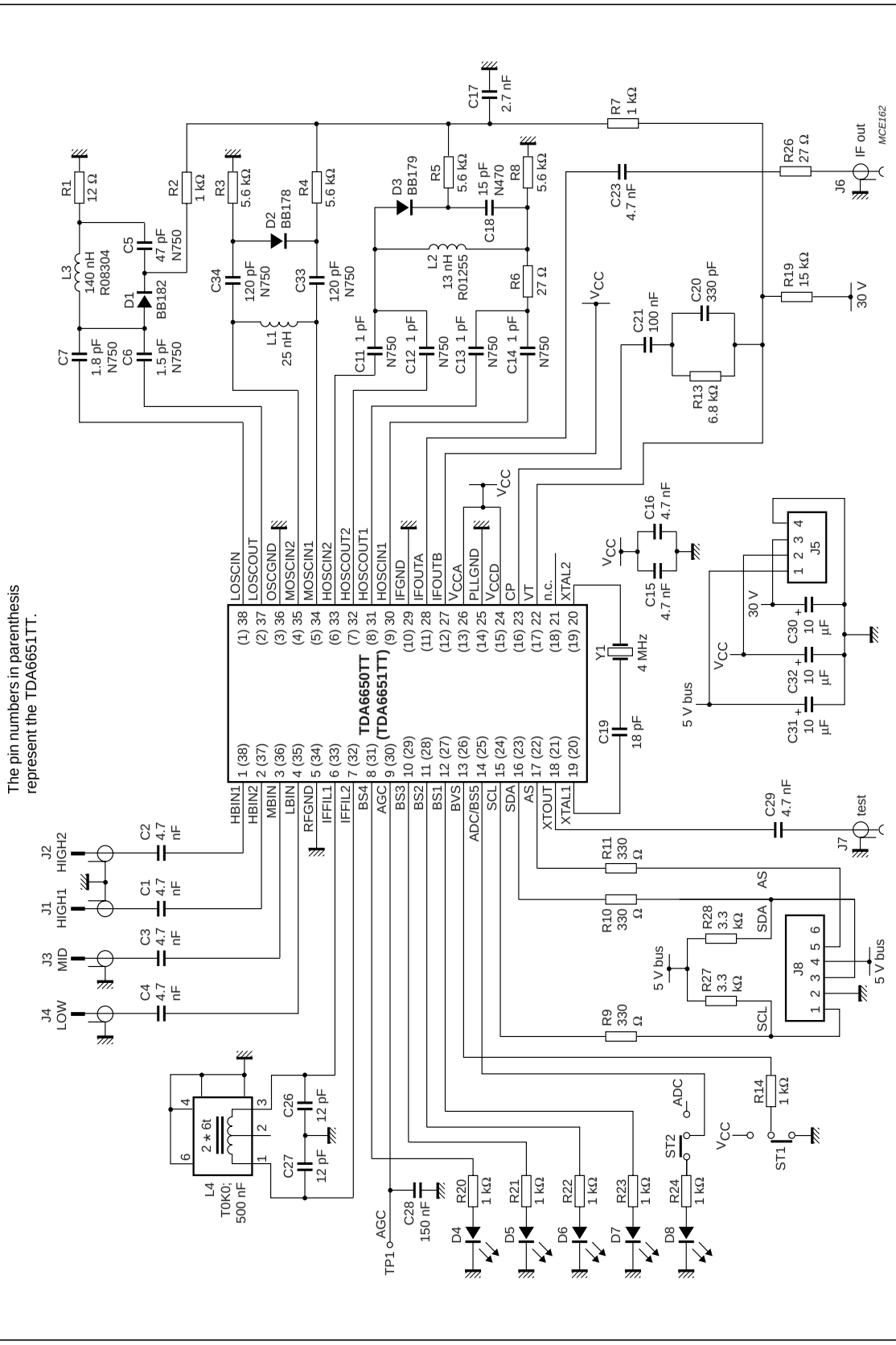


Fig.27 Measurement circuit for digital application, with asymmetrical IF output and DVB-T compliant loop filter.

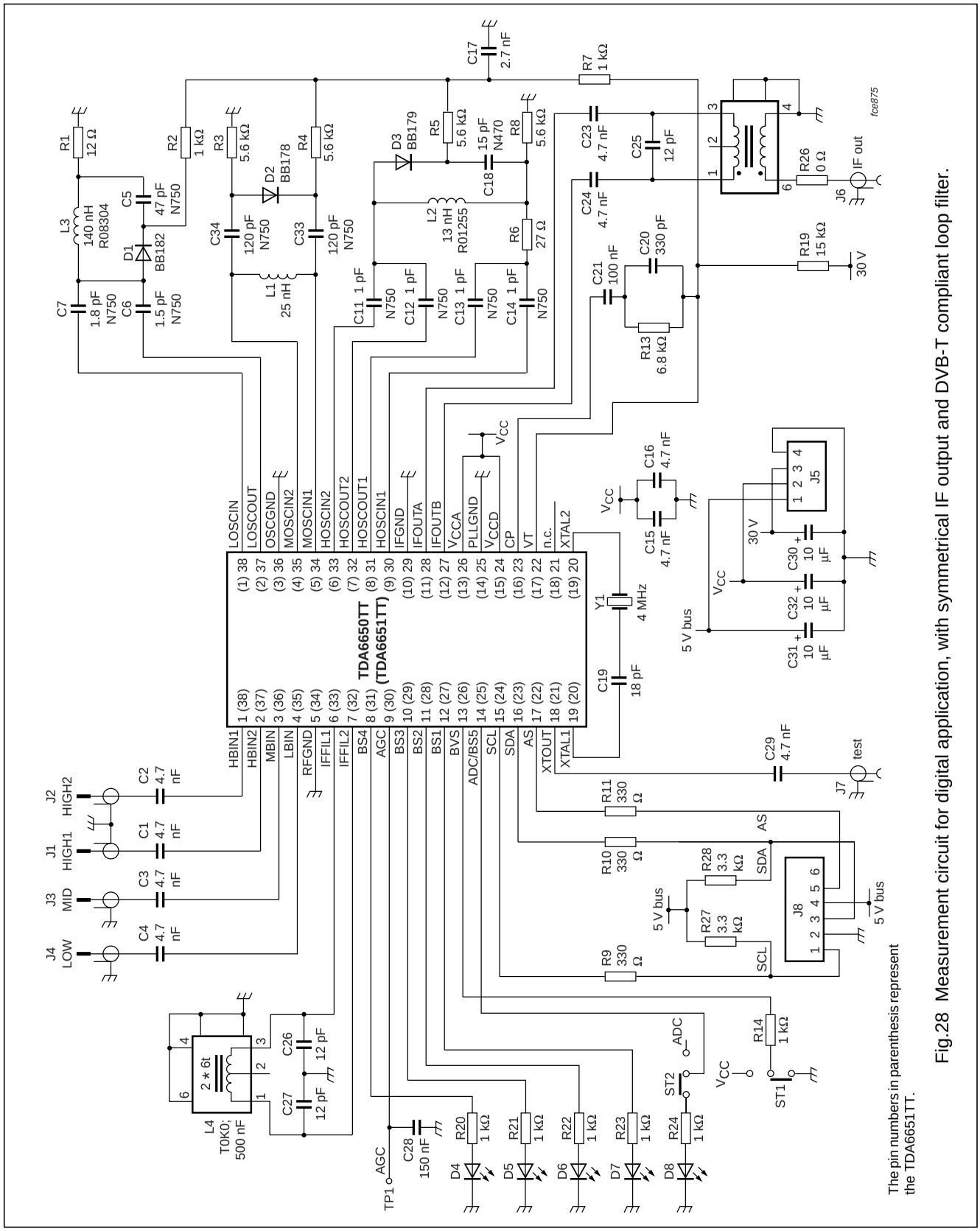


Fig.28 Measurement circuit for digital application, with symmetrical IF output and DVB-T compliant loop filter.

The pin numbers in parenthesis represent the TDA6651TT.

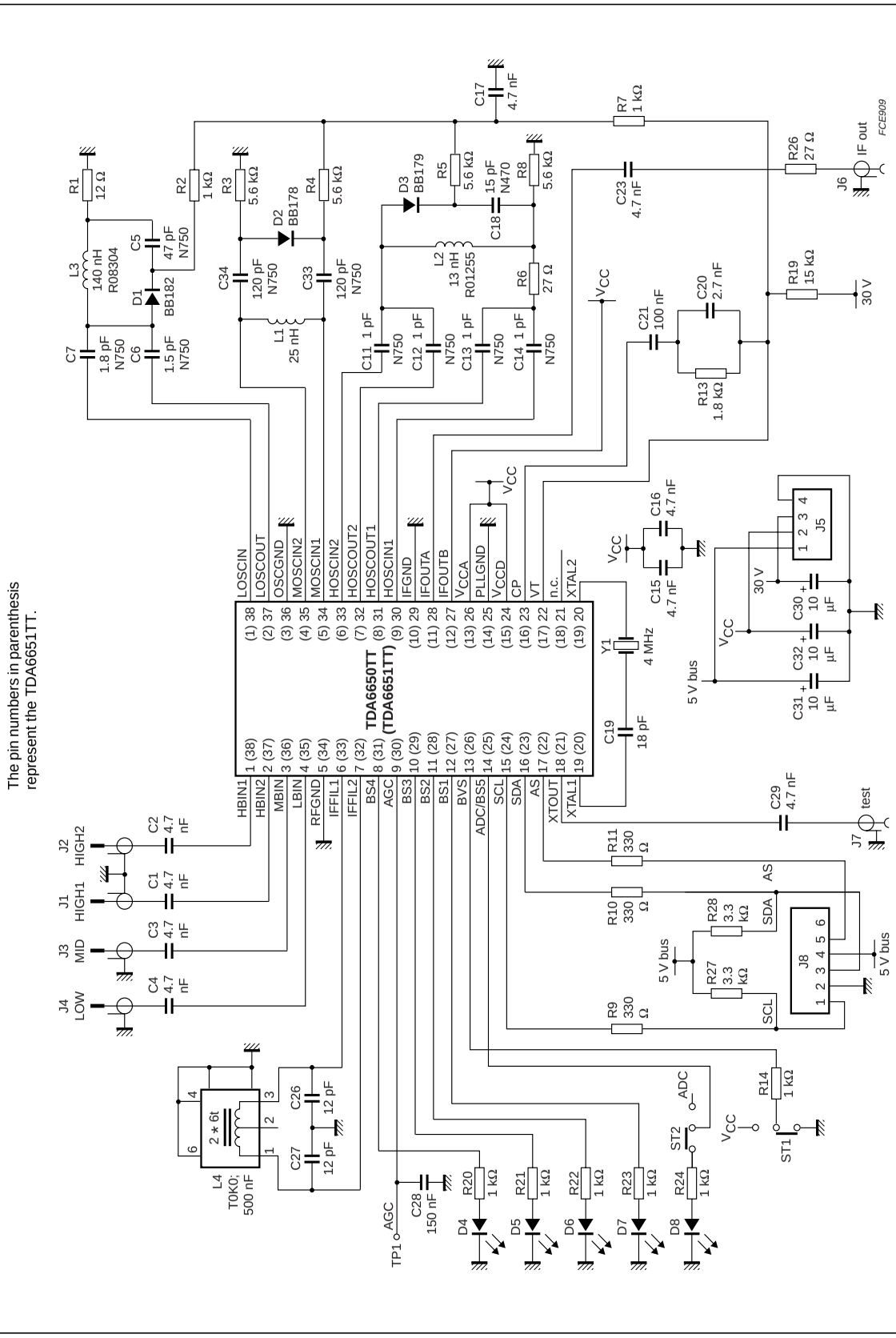


Fig.29 Measurement circuit for hybrid application, with asymmetrical IF output and loop filter for PAL and DVB-T standards.

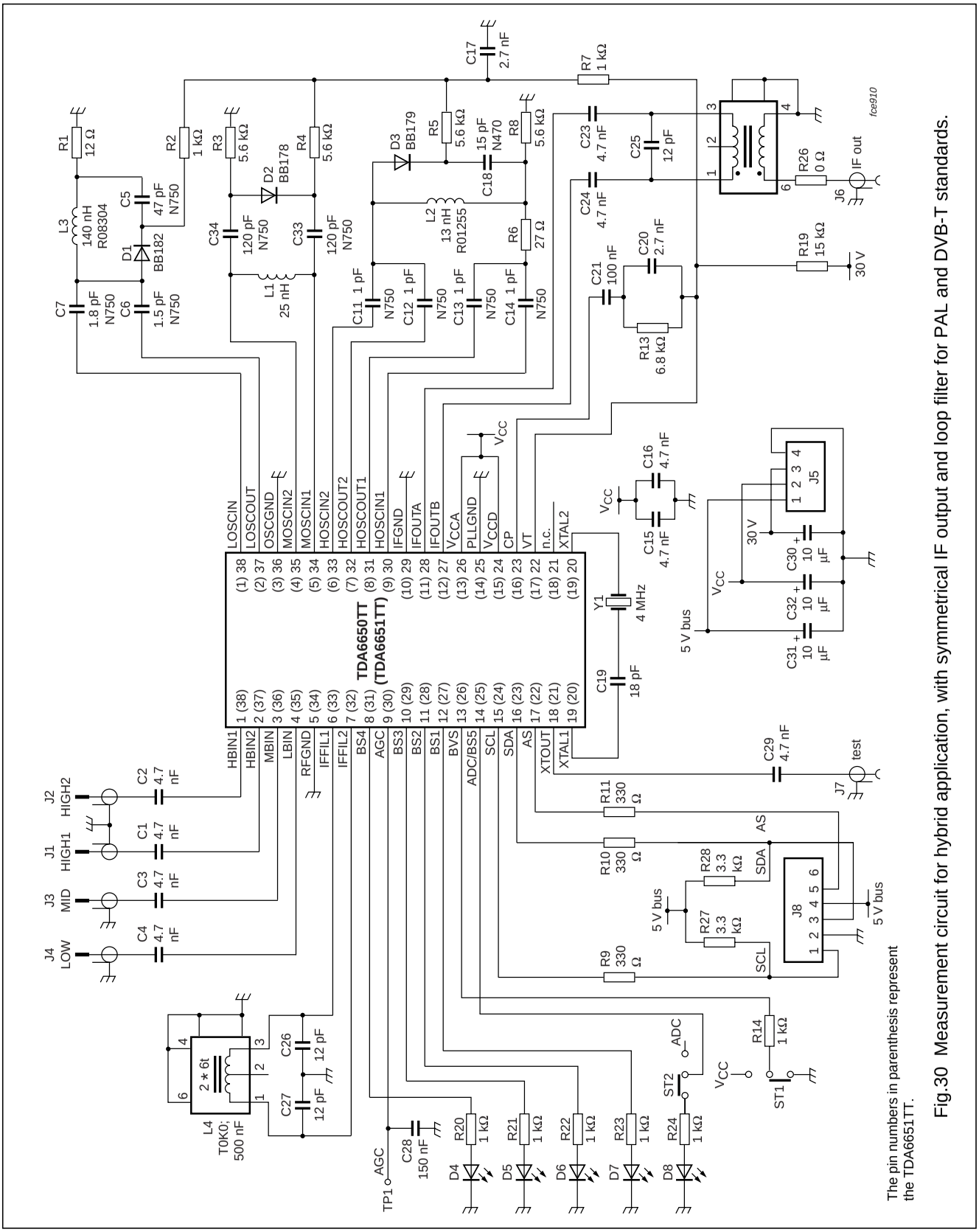
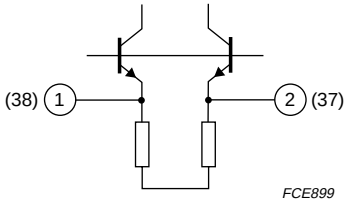
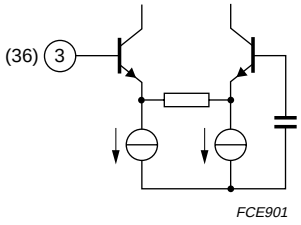
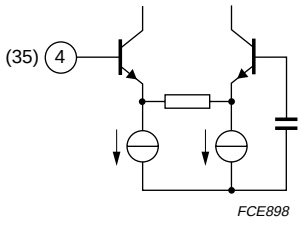
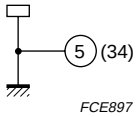
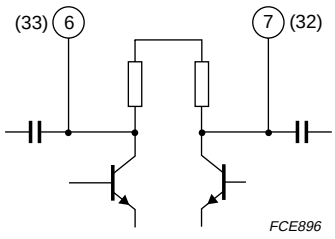
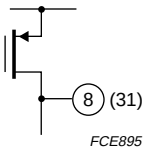
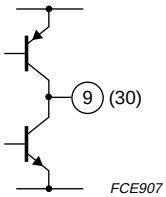
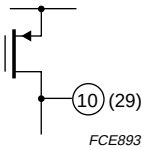
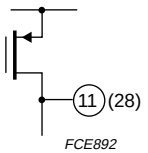
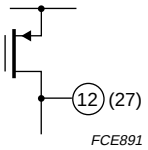


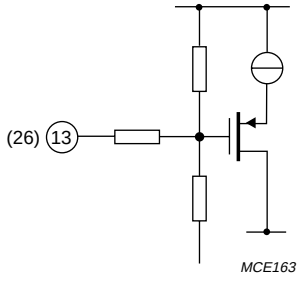
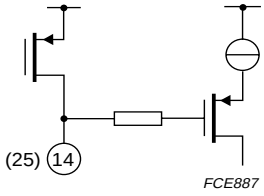
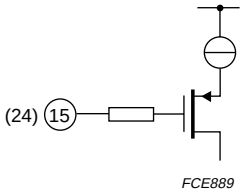
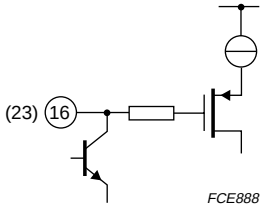
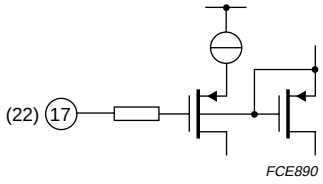
Fig.30 Measurement circuit for hybrid application, with symmetrical IF output and loop filter for PAL and DVB-T standards.

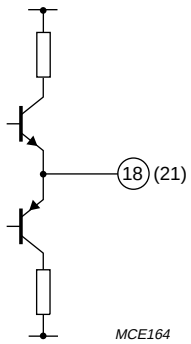
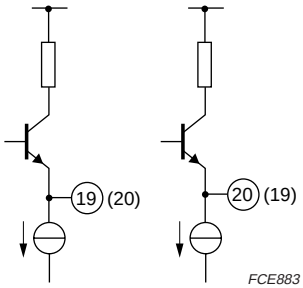
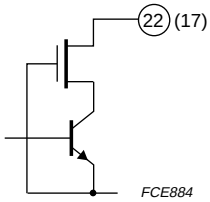
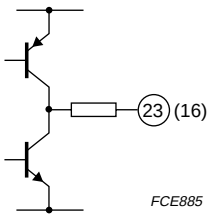
The pin numbers in parenthesis represent the TDA6651TT.

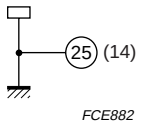
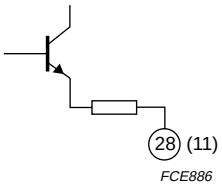
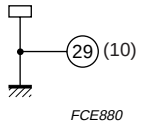
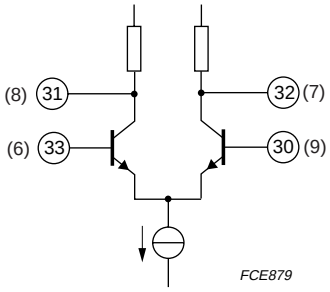
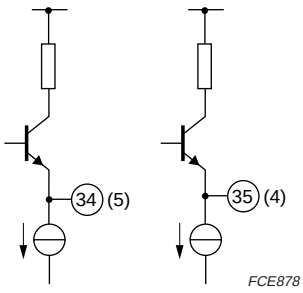
13 INTERNAL PIN CONFIGURATION

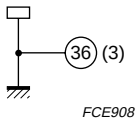
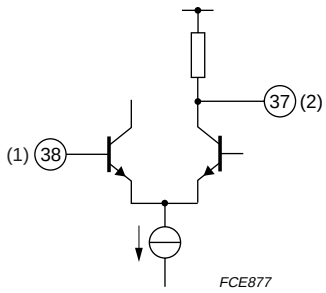
SYMBOL	PIN		AVERAGE DC VOLTAGE VERSUS BAND SELECTION			DESCRIPTION(1)
	TDA6650TT	TDA6651TT	LOW	MID	HIGH	
HBIN1	1	38	n.a.	n.a	1.0 V	
HBIN2	2	37	n.a.	n.a	1.0 V	
MBIN	3	36	n.a.	1.8 V	n.a.	
LBIN	4	35	1.8 V	n.a.	n.a	
RFGND	5	34	–	–	–	
IFFIL1	6	33	3.7 V	3.7 V	3.7 V	
IFFIL2	7	32	3.7 V	3.7 V	3.7 V	

SYMBOL	PIN		AVERAGE DC VOLTAGE VERSUS BAND SELECTION			DESCRIPTION(1)
	TDA6650TT	TDA6651TT	LOW	MID	HIGH	
BS4	8	31	high Z or $V_{CC} - V_{DS}$	high Z or $V_{CC} - V_{DS}$	high Z or $V_{CC} - V_{DS}$	
AGC	9	30	0 V or 3.5 V	0 V or 3.5 V	0 V or 3.5 V	
BS3	10	29	high Z or $V_{CC} - V_{DS}$	high Z or $V_{CC} - V_{DS}$	high Z or $V_{CC} - V_{DS}$	
BS2	11	28	high Z	$V_{CC} - V_{DS}$	high Z	
BS1	12	27	$V_{CC} - V_{DS}$	high Z	high Z	

SYMBOL	PIN		AVERAGE DC VOLTAGE VERSUS BAND SELECTION			DESCRIPTION(1)
	TDA6650TT	TDA6651TT	LOW	MID	HIGH	
BVS	13	26	2.5 V	2.5 V	2.5 V	
ADC/BS5	14	25	V_{CEsat} or high Z	V_{CEsat} or high Z	V_{CEsat} or high Z	
SCL	15	24	high Z	high Z	high Z	
SDA	16	23	high Z	high Z	high Z	
AS	17	22	1.25 V	1.25 V	1.25 V	

SYMBOL	PIN		AVERAGE DC VOLTAGE VERSUS BAND SELECTION			DESCRIPTION(1)
	TDA6650TT	TDA6651TT	LOW	MID	HIGH	
XTOUT	18	21	3.45 V	3.45 V	3.45 V	
XTAL1	19	20	2.2 V	2.2 V	2.2 V	
XTAL2	20	19	2.2 V	2.2 V	2.2 V	
n.c.	21	18	n.a.			not connected
VT	22	17	V_{VT}	V_{VT}	V_{VT}	
CP	23	16	1.8 V	1.8 V	1.8 V	
V_{CCD}	24	15	5 V	5 V	5 V	

SYMBOL	PIN		AVERAGE DC VOLTAGE VERSUS BAND SELECTION			DESCRIPTION(1)
	TDA6650TT	TDA6651TT	LOW	MID	HIGH	
PLLGND	25	14	–	–	–	
V_{CCA}	26	13	5 V	5 V	5 V	
IFOUTB	27	12	2.1 V	2.1 V	2.1 V	
IFOUTA	28	11	2.1 V	2.1 V	2.1 V	
IFGND	29	10	–	–	–	
HOSCIN1	30	9	2.2 V	2.2 V	1.8 V	
HOSCOUT1	31	8	5 V	5 V	2.5 V	
HOSCOUT2	32	7	5 V	5 V	2.5 V	
HOSCIN2	33	6	2.2 V	2.2 V	1.8 V	
MOSCIN1	34	5	2.3 V	1.3 V	2.3 V	
MOSCIN2	35	4	2.3 V	1.3 V	2.3 V	

SYMBOL	PIN		AVERAGE DC VOLTAGE VERSUS BAND SELECTION			DESCRIPTION(1)
	TDA6650TT	TDA6651TT	LOW	MID	HIGH	
OSCGND	36	3	–	–	–	
LOSCOUT	37	2	1.7 V	1.4 V	1.4 V	
LOSCIN	38	1	2.9 V	3.5 V	3.5 V	

Note

1. The pin numbers in parenthesis refer to the TDA6651TT.

14 APPLICATION AND TEST INFORMATION

14.1 Tuning amplifier

The tuning amplifier is capable of driving the varicap voltage without an external transistor. The tuning voltage output must be connected to an external load of 15 kΩ which is connected to the tuning voltage supply rail. The loop filter design depends on the oscillator characteristics and the selected reference frequency as well as the required PLL loop bandwidth.

Applications with the TDA6650TT; TDA6651TT have a large loop bandwidth, in the order of a few tens of kHz. The calculation of the loop filter elements has to be done for each application, it depends on the reference frequency and charge pump current. A simulation of the loop can easily be done using the SIMPATA software from Philips.

14.2 Crystal oscillator

The TDA6650TT; TDA6651TT needs to be used with a 4 MHz crystal in series with a capacitor with a typical value of 18 pF, connected between pin XTAL1 and pin XTAL2. Philips crystal 4322 143 04093 is recommended. When choosing a crystal, take care to select a crystal able to withstand the drive level of the TDA6650TT; TDA6651TT without suffering from accelerated ageing. For optimum performances, it is highly recommended to connect the 4 MHz crystal without any serial resistance.

The crystal oscillator of the TDA6650TT; TDA6651TT should not be driven (forced) from an external signal.

Do not use the signal on pins XTAL1 or XTAL2, or the signal present on the crystal, to drive an external IC or for any other use as this may dramatically degrade the phase noise performance of the TDA6650TT; TDA6651TT.

14.3 Examples of I²C-bus program sequences

Tables 16 to 23 show various sequences where:

S = START

A = acknowledge

P = STOP.

The following conditions apply:

LO frequency is 800 MHz

f_{comp} = 166.666 kHz

N = 4800

BS3 output port is on and all other ports are off: thus the high band is selected

Charge pump current I_{CP} = 280 μA

Normal mode, with XTOUT buffer on

I_{AGC} = 220 nA

AGC take-over point is set to 112 dBμV (p-p)

Address selection is adjusted to make address C2 valid.

To fully program the device, either sequence of Table 16 or 17 can be used, while other arrangements of the bytes are also possible.

Table 16 Complete sequence 1

START	ADDRESS BYTE		DIVIDER BYTE 1		DIVIDER BYTE 2		CONTROL BYTE 1(1)		CONTROL BYTE 2		CONTROL BYTE 1(2)		STOP
S	C2	A	12	A	C0	A	CA	A	A4	A	84	A	P

Notes

1. Control byte 1 with bit T/A = 1, to program test bits T2, T1 and T0 and reference divider ratio bits R2, R1 and R0.
2. Control byte 1 with bit T/A = 0, to program AGC time constant bit ATC and AGC take-over point bits AL2, AL1 and AL0.

Table 17 Complete sequence 2

START	ADDRESS BYTE		CONTROL BYTE 1(1)		CONTROL BYTE 2		DIVIDER BYTE 1		DIVIDER BYTE 2		CONTROL BYTE 1(2)		STOP
S	C2	A	CA	A	A4	A	12	A	C0	A	84	A	P

Notes

1. Control byte 1 with bit T/A = 1, to program test bits T2, T1 and T0 and reference divider ratio bits R2, R1 and R0.
2. Control byte 1 with bit T/A = 0, to program AGC time constant bit ATC and AGC take-over point bits AL2, AL1 and AL0.

Table 18 Sequence to program only the main divider ratio

START	ADDRESS BYTE		DIVIDER BYTE 1		DIVIDER BYTE 2		STOP
S	C2	A	12	A	C0	A	P

Table 19 Sequence to change the charge pump current, the ports and the test mode. If the reference divider ratio is changed, it is necessary to send the DB1 and DB2 bytes

START	ADDRESS BYTE		CONTROL BYTE 1(1)		CONTROL BYTE 2		STOP
S	C2	A	CA	A	A4	A	P

Note

1. Control byte 1 with bit T/A = 1, to program test bits T2, T1 and T0 and reference divider ratio bits R2, R1 and R0.

Table 20 Sequence to change the test mode. If the reference divider ratio is changed, it is necessary to send the DB1 and DB2 bytes

START	ADDRESS BYTE		CONTROL BYTE 1(1)		STOP
S	C2	A	CA	A	P

Note

1. Control byte 1 with bit T/A = 1, to program test bits T2, T1 and T0 and reference divider ratio bits R2, R1 and R0.

Table 21 Sequence to change the charge pump current, the ports and the AGC data

START	ADDRESS BYTE		CONTROL BYTE 1(1)		CONTROL BYTE 2		STOP
S	C2	A	82	A	A4	A	P

Note

1. Control byte 1 with bit T/A = 0, to program AGC time constant bit ATC and AGC take-over point bits AL2, AL1 and AL0.

Table 22 Sequence to change only the AGC data

START	ADDRESS BYTE		CONTROL BYTE 1(1)		STOP
S	C2	A	84	A	P

Note

1. Control byte 1 with bit T/A = 0, to program AGC time constant bit ATC and AGC take-over point bits AL2, AL1 and AL0.

Table 23 Sequence to program the main divider, the ALBC on and the test modes in normal mode with XTOUT buffer off.

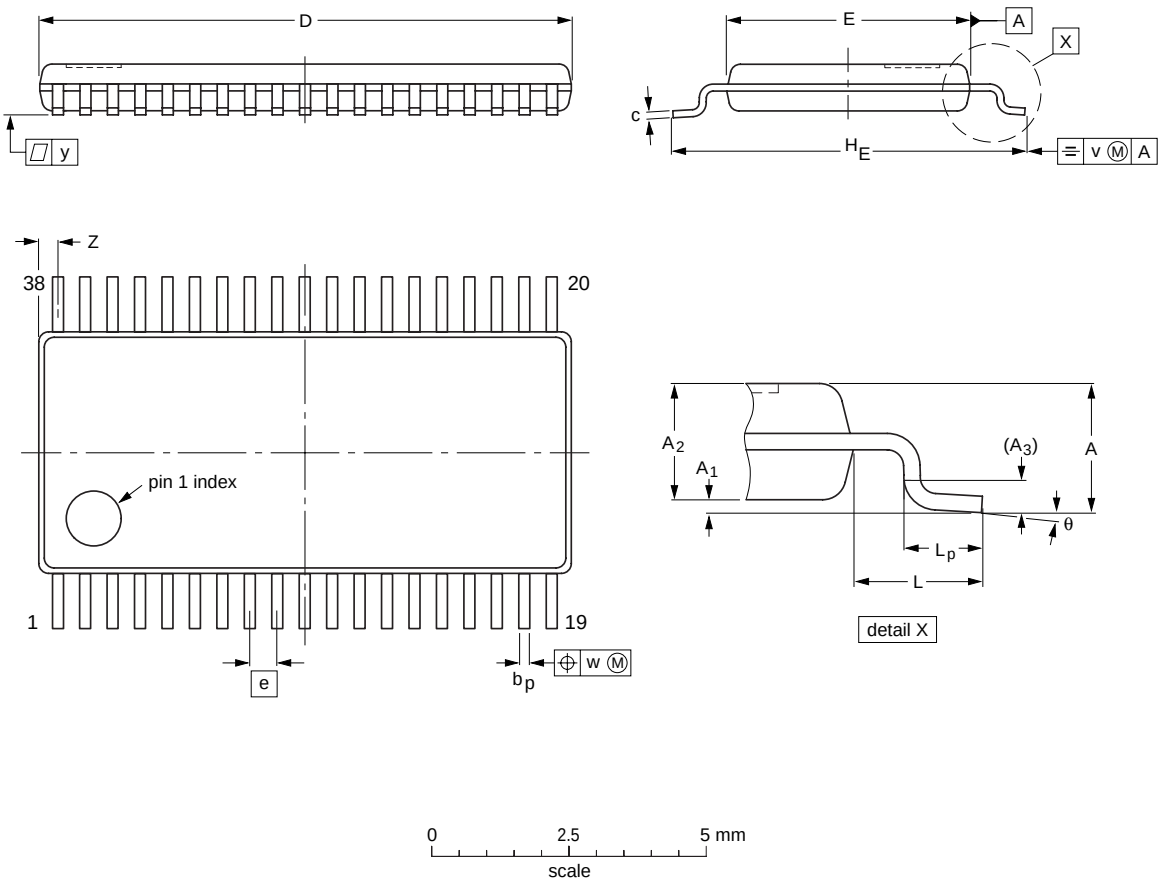
START	ADDRESS BYTE		DIVIDER BYTE 1		DIVIDER BYTE 2		CONTROL BYTE 1(1)		CONTROL BYTE 2		CONTROL BYTE 1		STOP
S	C2	A	12	A	C0	A	DA	A	00	A	C2	A	P

Note

1. Control byte 1 with bit T/A = 1, to program test bits T2, T1 and T0 and reference divider ratio bits R2, R1 and R0.

15 PACKAGE OUTLINE

TSSOP38: plastic thin shrink small outline package; 38 leads; body width 4.4 mm; lead pitch 0.5 mm **SOT510-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.85	0.25	0.27 0.17	0.20 0.09	9.8 9.6	4.5 4.3	0.5	6.4	1	0.7 0.5	0.2	0.08	0.08	0.49 0.21	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT510-1						~~98-09-16~~ 03-02-18

16 SOLDERING

16.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

16.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON-T and SSOP-T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

16.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

16.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

16.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, USON, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
4. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
5. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
6. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
7. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
8. Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
9. Hot bar or manual soldering is suitable for PMFP packages.

17 DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Notes

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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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