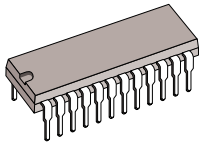
SGS-THOMSON MICROELECTRONICS

M34116

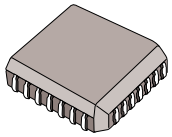
PCM CONFERENCE CALL AND TONE GENERATION CIRCUIT

PRELIMINARY DATA

- HW AND SW COMPATIBLE WITH M116
- 1 TO 64 SERIAL CHANNELS PER FRAME (CONTROLLED BY SYNC SIGNAL PERIOD)
- 29 MAXIMUM CONFERENCES
- 1 TO 64 SERIAL CHANNELS PER CONFERENCES
- 3 SIMULTANEOUS OPERATION MODES AVAILABLE:
  CONFERENCE, TRANSPARENT AND TONE GENERATION
- TYPICAL BIT RATES:
  1536/1544/2048/4096 Kbits/s
- COMPATIBLE WITH ALL KINDS OF PCM FORMAT
- μ AND A LAW (PIN PROGRAMMABLE)
- EQUAL PRIORITY TO EVERY CHANNEL
- ONE FRAME AND ONE CHANNEL DELAY FROM SENDING TO RECEIVING
- OVERFLOW INFORMATION FOR EACH CONFERENCE BY PIN OS (OVERFLOW SIGNALLING) AND ON DATA BUS ON MPU REQUEST
- INSTRUCTION SET COMPATIBLE WITH M3488
- PROGRAMMABLE INPUT AND OUTPUT ATTENUATION OR GAIN FROM 0 TO 15dB WITH STEP OF 1dB FOR EACH CHANNEL
- TONE GENERATION FROM 3.9Hz TO 3938Hz WITH MIN. STEP OF 3.9Hz
- TOTAL OF 7 DIFFERENT TONE OUTPUTS IN PARALLEL PROGRAMMABLE VIA MPU (MAXIMUM 4 DIFFERENT FREQUENCIES AND DURATIONS)
- 1 MELODY OF MAXIMUM 32 PROGRAMMABLE FREQUENCIES AND DURATIONS
- 5V POWER SUPPLY
- TTL COMPATIBLE INPUT LEVELS, CMOS/TTL COMPATIBLE OUTPUT LEVELS
- MAIN INSTRUCTIONS CONTROLLED BY MICROPROCESSOR INTERFACE:
  – Channel connection to a conference
  – Channel attenuation or gain
  – Channel disconnection from both conference and transparent modes
  – Tone and melody generation
  – Overflow status
  – Operating mode
  – Channel status



DIP24
ORDERING NUMBER: M34116B1



PLCC28
ORDERING NUMBER: M34116C1

DESCRIPTION

The M34116 is a product specifically designed for applications in PCM digital exchanges. It is able to handle up to 64 channels in any conferences combination from 1 to 29 conferences in parallel and to generate seven different tones and one melody.

The parties in a conference must previously be allocated through the Digital Switching Matrix (M3488) in a single serial wire at M34116 PCM input (IN PCM pin).

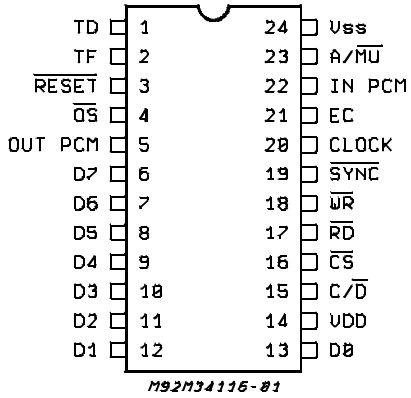
The M34116 is full pin and function compatible with the M116. In addition, it has the capability to generate tone directly coded in PCM.

For the conference function, each channel is converted inside the chip from PCM law to linear law (14 bits). Then it is added to its conference, and the sample of the previous frame is subtracted from the conference.
In this way a new conference sum signal is generated.
The channel output signal will contain the information of all the other channels in its conference except its own.

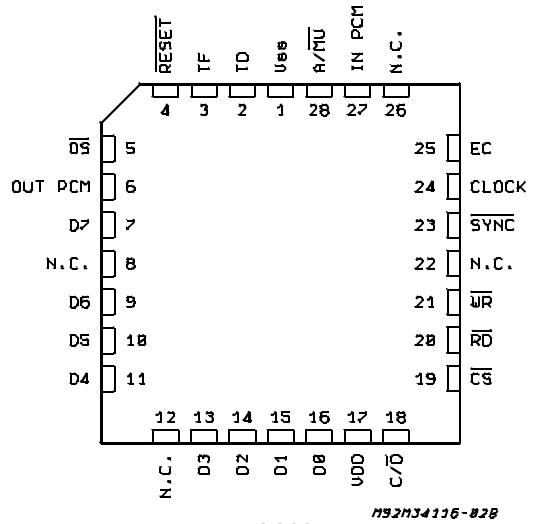
After the PCM encoding, the data is serialized by the M34116 in the same sequence as the PCM input frame, with one frame (plus one channel) delay and will be reallocated by the DSM (M3488) at the final channel and bus position.

A programmable attenuation or gain can be set on each channel and for every function: conference, tone generation and transparent mode.

PIN CONNECTIONS (Top view)



DIP24



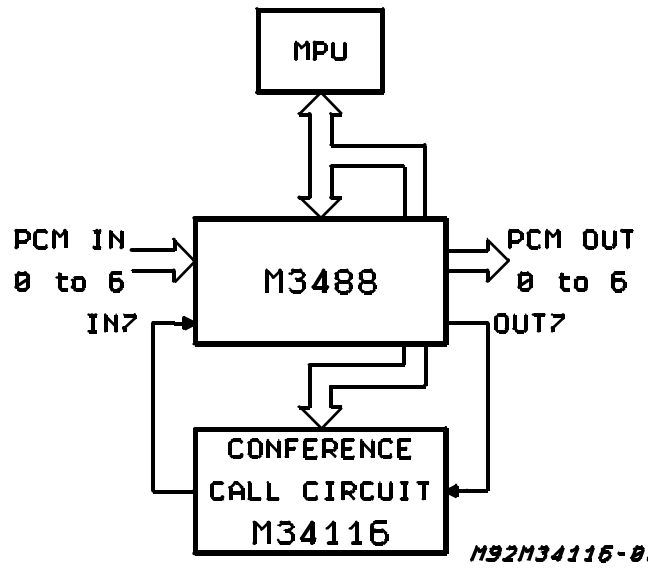
PLCC28

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD} (*)	Supply Voltage	– 0.3 to 7	V
V_i	Input Voltage	– 0.3 to V_{DD}	
$V_{O\ (off)}$	Off State Output Voltage	– 0.3 to 7	V
P_{tot}	Total Power Dissipation	500	mW
T_{stg}	Storage Temperature	– 65 to 150	°C
T_{op}	Operating Temperature	0 to 70	°C

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 1: PCM Conference Call Insertion Scheme



PIN DESCRIPTION

DIP N°	PLCC N°	Pin	Function
1	2	TD	M116 operating mode only. Tone Duration input pin. When TD = 1, a PCM coded tone (instead of PCM data) is sent out to all channels enabled by the IT bit. TD is latched by the SYNC signal so that all channels have the same tone during the same number of frames. TD = 0 for normal operation.
2	3	TF	M116 operating mode only. Tone Frequency input pin. When TF = 1, the tone amplitude is high. When TF = 0, the tone amplitude is low. TF is latched by SYNC. The PCM coded tone level corresponds to 1/10 of the full scale. For M34116 operating mode: Melody waveform select input pin. When TF = 1, the PCM output of the melody represents a square wave. When TF = 0, it represents a sine wave. In both cases, the rms level is the same and is equal to – 6 dBm0 if no attenuation or gain is programmed.
3	4	$\overline{\text{RESET}}$	Master reset input pin. This pin is active low and must be used at the very beginning after power up to initialize the device or when switching from A law to Mu law. The Internal initialization routine takes 2 time frames starting from the rising edge of RESET. During this initialization time, all data bus and PCM output are pulled to a high impedance state.
4	5	$\overline{\text{OS}}$	Overflow Signalling output pin. When $\overline{\text{OS}}$ = 0 one conference is in overflow. This signal is anticipated over half time slot with respect to the output channel involved in the conference in overflow. Example: if output channel 4 is one of the parties of one conference in overflow, $\overline{\text{OS}}$ = 0 during the second half of the time slot corresponding to output channel 3 and during the first half of the time slot corresponding to output channel 4.
5	6	OUT PCM	PCM output pin. The bit rate is 4096Kbits/s max. The sign bit is the first bit of the serial sequence. The first bit of the first channel is found at the rising edge of the CLOCK signal preceding the rising edge of the SYNC signal. The output buffer is open drain to allow for multiple connections.
6 to 13	7, 9 to 11, 13 to 16	D0 to D7	Bidirectional Data bus pins. Data and instructions are transferred to or from the microprocessor. D0 is the Least Significant Bit. The bus is tristate when RESET is low and/or $\overline{\text{CS}}$ is high.
14	17	VDD	+5V Supply input. 100nF decoupling capacitor recommended.
15	18	C/$\overline{\text{D}}$	Control Data input pin. In a write operation C/$\overline{\text{D}}$ = 0 qualifies any bus content as data while C/D = 1 qualifies it as an opcode. For M116 operating mode only: in a read operation, the overflow information of the first eight conferences is selected by C/D = 0, the overflow of the last two conferences and the status by C/D = 1.
16	19	$\overline{\text{CS}}$	Chip Select input pin. When $\overline{\text{CS}}$ = 0, data and instructions can be transferred to or from the external microprocessor and when $\overline{\text{CS}}$ = 1 the data bus is in tristate.
17	20	$\overline{\text{RD}}$	Read control input pin. When $\overline{\text{RD}}$ = 0, read operation is performed. When match conditions for the opcode exists, data is transferred to the external microprocessor on the falling edge of $\overline{\text{RD}}$.
18	21	$\overline{\text{WR}}$	Write control input pin. Instructions and opcode from the external microprocessor are latched on the rising edge of $\overline{\text{WR}}$.
19	23	$\overline{\text{SYNC}}$	Synchronization input pin. The rising edge of CLOCK preceding the rising edge of $\overline{\text{SYNC}}$ corresponds to the first bit of the first channel except for PCM frame of 1544Kbits/s. In this case, it corresponds to the Extra bit (193th).
20	24	CLOCK	Master Clock input pin. Typ. operating Frequencies are: 3.072MHz for 24 PCM channels frame (192 bit/frame) 3.088MHz for 24 PCM channels frame with extra bit (193 bit/frame) 4.096MHz for 32 PCM channels frame (256 bit/frame) 8.192MHz for 64 PCM channels frame (512 bit/frame) Both M34116 an M116 operating modes are possible up to 4.096MHz. At 8.192MHz only M34116 operating mode is possible.
21	25	EC	External Clock output pin. This pin provides the master clock for the Digital Switching Matrix (M3488). Normally it is the same signal as applied to the CLOCK input (pin 20). When the Extra bit is selected with the instruction 5, the first two periods of the master clock are canceled in order to allow the operation of the M34116 and the DSM with PCM frame with Extra bit (e.g. 193 bit/frame with PCM I/O of 1544Kbits/s).
22	27	IN PCM	PCM input pin. The max bit rate is 4096Kbits/s. The first bit of the first cahnnel is found at the second rising edge of the CLOCK signal following the rising edge of the SYNC signal. If Extra bit is selected, then the first bit is shifted by two CLOCK periods.
23	28	A/$\overline{\text{MU}}$	A Law or MU Law select pin. When A/$\overline{\text{MU}}$ = 1, A Law is selected. When A/$\overline{\text{MU}}$ = 0, MU Law is selected. The law selection must be done before initializing the device using the $\overline{\text{RESET}}$ pin.
24	1	Vss	Ground.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.75 to 5.25	V
V_i	Input Voltage	0 to 5.25	V
V_O	Off State Output Voltage	0 to 5.25	V
CLOCK Freq.	Input Clock Frequency	3.072/3.088 4.096 / 8.192 (*)	MHz MHz
$\overline{SYNC}$ Freq.	Input Synchronization Frequency	8	KHz
T_{op}	Operating Temperature	0 to 70	°C

CAPACITANCES (measurements frequency = 1MHz; 0 to 70°C; unused pins tied to V_{SS})

Symbol	Parameter	Pin (**)	Min.	Typ.	Max.	Unit
C_I	Input Capacitance	1 to 3; 15 to 20; 22 to 23			5	pF
$C_{I/O}$	I/O Capacitance	6 to 13			15	pF
C_O	Output Capacitance	4, 5, 21			10	pF

ELECTRICAL CHARACTERISTICS (Tamb = 0 to 70°C, V_{CC} = 5V ± 5%)
All DC characteristic are valid 250µs after V_{CC} and clock have been applied.

Symbol	Parameter	Pins (**)	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level	1 to 3 15 to 20 22 to 23		– 0.3		+0.8	V
V_{IH}	Input High Level	1 to 3 15 to 20 22 to 23		2.0		V_{CC}	V
V_{T-}	Negative Threshold Voltage	6 to 13 (***)	V_{CC} = 5V	0.6	0.9	1.1	V
V_{T+}	Positive Threshold Voltage	6 to 13 (***)	V_{CC} = 5V	1.5	1.7	2	V
V_{HY}	Hysteresis	6 to 13 (***)	V_{CC} = 5V	0.4	0.8		V
V_{OL}	Output Low Level	4,6 to 13,21	I_{OL} = 2mA			0.4	V
V_{OH}	Output High Level	4 to 13, 21	I_{OH} = 1mA	V_{CC}-0.4			V
V_{OL}	Output Low Level	5	I_{OL} = 4.1mA			0.4	V
I_{IL}	Input Leakage Current	1 to 3 6 to 13 15 to 20 22 to 23	V_{IN} = 0 to V_{CC}			10	µA
I_{OL}	Data Bus Leakage Current	6 to 13	$\underline{V_{IN}}$ = 0 to V_{CC} CS = V_{CC}			±10	µA
I_{CC}	Supply Current	14	Clock Freq. = 4.096MHz			50	mA

(*) Only in M34116 Operating Mode.
(**) Pin numbers referred to the DIP24.
(***) Schimitt-trigger inputs.

ELECTRICAL CHARACTERISTICS (Tamb = 0 to 70°C, V_{CC} = 5V ± 5%)
All DC characteristic are valid 250µs after V_{CC} and clock have been applied. C_L is the max. capacitive load and R_L the test pull up resistor.

Signal	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
CK Up to 4.096MHz	t_{CK}	Clock Period		230			ns
	t_{WL}	Clock Low Level Width		100			ns
	t_{WH}	Clock High Level Width		100			ns
	t_R	Rise Time				25	ns
	t_F	Fall Time				25	ns
CK 8.192MHz	t_{CK}	Clock Period		120			ns
	t_{WL}	Clock Low Level Width		50			ns
	t_{WH}	Clock High Level Width		50			ns
	t_R	Rise Time				10	ns
	t_F	Fall Time				10	ns
$\overline{SYNC}$	t_{SL}	Low Level Set-up Time	See note 1	30			ns
	t_{HL}	Low Level Hold Time		30			ns
	t_{SH}	High Level Set-up Time		30			ns
	t_{WH}	High Level Width		t_{CK}			ns
PCM Input	t_S	Set-up Time		35			ns
	t_H	Hold Time		35			ns
PCM Output (Open drain)	$t_{PD\ min.}$	Propagation Time Low Level referred to CK	C_L = 50pF R_L = 1KΩ	40			ns
	$t_{PD\ max.}$	Propagation Time High level Referred to CK				180	ns
$\overline{RESET}$	t_{SL}	Low Level Set-up Time	note 6	50			ns
	t_{HL}	Low Level Hold Time		30			ns
	t_{SH}	High Level Set-up Time		30			ns
	t_{WH}	High Level Width		t_{CK}			ns
$\overline{WR}$	t_{WL}	Low Level Width		150			ns
	t_{WH}	High Level Width		200			ns
	t_{REP}	Repetition interval between active pulses.	note 3 and 4	500			ns
	t_{SH}	High Level st-up time to active read strobe.		0			ns
	t_{HH}	High Level hold time to active read strobe.		20			ns
	t_R	Rise Time				60	ns
	t_F	Fall Time				60	ns
RD	t_{WL}	Low Level Width		180			ns
	t_{WH}	High Level Width		200			ns
	t_{REP}	Repetition interval between active pulses.	note 5	4 t_{CK}			ns
	t_{SH}	High Level st-up time to active read strobe.		0			ns
	t_{HH}	High Level hold time to active read strobe.		20			ns
	t_R	Rise Time				60	ns
	t_F	Fall Time				60	ns

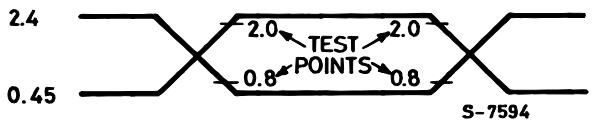
Notes:

1. With Extra Bit operating mode insert this time becomes 3 t_{CK}.
2. With Extra Bit operating mode insert these times are 80ns longer.
3. With OPCODE (C/D = I), this time becomes 4tck (6tck if E = 1). E: extra bit indication in "operating mode" instruction.
4. For tone generation instruction, this time becomes 4tck (6tck if E = 1) E: extra bit indication in "operating mode" instruction.
5. With extra bit operating mode insert, this time becomes 6tck.
6. The initialization routine takes 2 frames time starting from the rising edge of $\overline{RESET}$ - Any access to the device should take place after the initialization routine is completed. (2 frames time).

ELECTRICAL CHARACTERISTICS (continued)

Signal	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$\overline{CS}$	$t_{SL\ (\overline{CS}\text{-}\overline{WR})}$	Low level set-up time to WR falling edge.	Active Case	0			ns
	$t_{HL\ (\overline{CS}\text{-}\overline{WR})}$	Low Level hold time from WR rising edge.	Active Case	20			ns
	$t_{SH\ (\overline{CS}\text{-}\overline{WR})}$	High level set-up time to WR falling edge.	Inactive Case	0			ns
	$t_{HH\ (\overline{CS}\text{-}\overline{WR})}$	High level hold time from WR rising edge.	Inactive Case	20			ns
	$t_{SL\ (\overline{CS}\text{-}\overline{RD})}$	Low level set-up time to RD falling edge.	Active Case	0			ns
	$t_{HL\ (\overline{CS}\text{-}\overline{RD})}$	Low Level hold time from RD rising edge.	Active Case	0			ns
	$t_{SH\ (\overline{CS}\text{-}\overline{RD})}$	High level set-up time to RD falling edge.	Inactive Case	0			ns
	$t_{HH\ (\overline{CS}\text{-}\overline{RD})}$	High level hold time from RD rising edge.	Inactive Case	0			ns
$\overline{CD}$	$t_{S(\overline{C/D}\text{-}\overline{WR})}$	Set-up time to write strobe end.		130			ns
	$t_{H(\overline{C/D}\text{-}\overline{WR})}$	Hold time from write strobe end.		25			ns
	$t_{S(\overline{C/D}\text{-}\overline{RD})}$	Set-up time to read strobe start.		20			ns
	$t_{H(\overline{C/D}\text{-}\overline{RD})}$	Hold time from read strobe end.		25			ns
$\overline{OS}$	$t_{PD(\overline{OS})}$	Propagation time from rising edge of CK.	C_L = 50pF			100	ns
EC	$t_{PD(EC)}$	Propagation time referred to CK edges.	C_L = 50pF			30	ns
TD/TF	t_S t_H	Set-up Hold Time		80 40			ns ns
D0 to D7 (interface bus)	$t_{S(BUS-WR)}$	Input set-up time to write strobe end.		130			ns
	$t_{H(BUS-WR)}$	Input hold time from write strobe end.		25			ns
	$t_{PD(BUS)}$	Propagation time from (active) falling edge of read strobe.	CL = 200pF			120	ns
	$t_{HZ(BUS)}$	Propagation time from (active) rising edge of read strobe to high impedance state.				80	ns

A.C. TESTING, OUTPUT WAVEFORM



A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0", timing measurement are made at 2.0V for a logic "1" and 0.8V for a logic "0".

Figure 2: Insertion Schema of M34116 in a 480 x 480 Non-Blocking Digital Switching Matrix

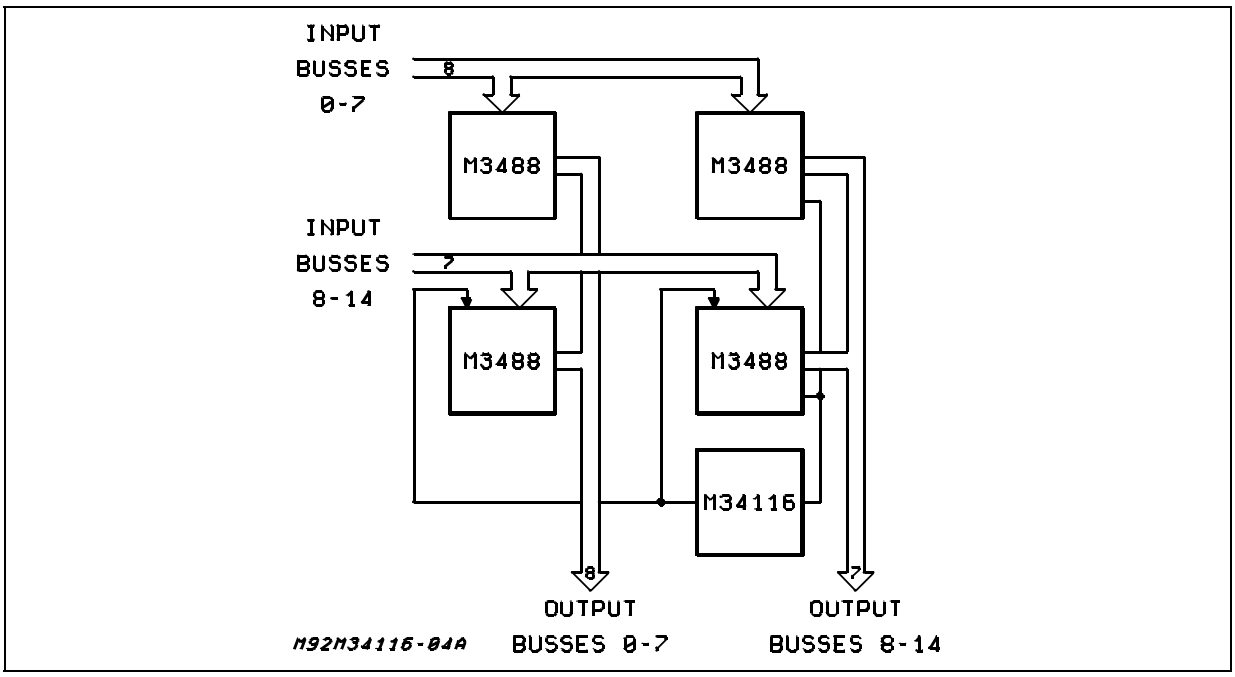
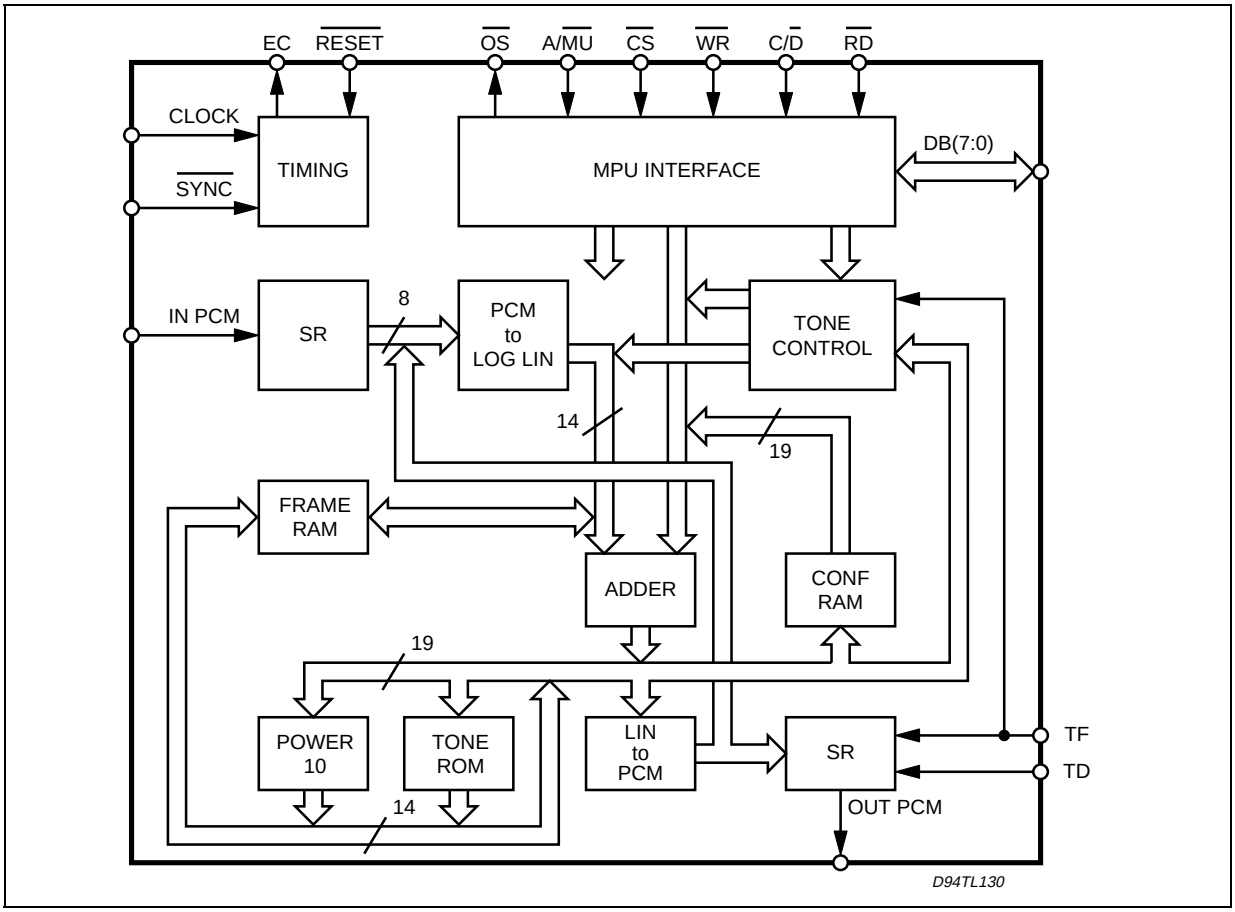


Figure 3: Block Diagram



CIRCUIT DESCRIPTION

ALGORITHMS

- Conference. For each channel, the PCM signal coming in is added to its conference and the PCM signal of the previous frame is subtracted to its conference before being sent out. The output signal contains only the data of all the other channels in its conference except its own.
- Tone. A fourth of a sine wave equivalent to 3.9Hz (8KHz/2048) is stored in a ROM which is read at multiple of the step (modulus 512) equivalent to the specified frequency. This step is used until the duration is reached then a new step will be used according to the specified sequence.
- Attenuation gain. The PCM signal is converted to logarithmic of the equivalent linear and then added or subtracted to the specified level. It is then raised to the power of 10 to be converted back to linear.

ARCHITECTURE

The basic time slot (16 periods of the master clock) is divided in four different parts that perform four different operations (also refer to Fig. 2 block diagram):

input processing: attenuation or gain of input PCM according to the algorithm mentioned earlier. The serial PCM signal coming in is loaded as 8 bits parallel and converted to logarithmic of the linear (through the PCM to LOG LIN block). It is then added to the attenuation or gain levels (also in logarithmic) stored in the MPU interface, the result is raised to the power of 10 (through the POWER 10 block) to be converted back to linear and written in the FRAME RAM.

conference addition: the above PCM signal, amplified or attenuated and converted in linear, is added to the conference and the result is stored in the conference RAM (block CONF RAM).

conference subtraction: the signal stored in the FRAME RAM during the previous frame is subtracted to the conference and the result is stored in the conference RAM.

output processing: attenuation or gain of the PCM to be sent out. The result of the above substraction is converted to PCM (through the block LIN to PCM) and to logarithmic (through the block PCM to LOG LIN), added to the attenuation or gain level stored in the MPU interface, converted to linear (through the block POWER 10) and then to PCM (through the block LIN to PCM). The resulting 8 bits are then shifted out serially.

If a channel is in conference, then all the four above operations are applied. If it is in transparent mode, then only the first and last operations are applied. For tone generation, the two first operations are not used. During the third part, the tone ROM is read. Since the ROM data is in linear it can therefore be applied to the fourth operation for output processing.

By default, after reset, the M34116 has the functionality and the instruction set of the M116. With a new operating mode instruction, the user can select the functionality of the M34116 with its new instruction set. The instruction set includes:

◊ operating mode: the user can choose either the M116 mode or the M34116 mode, the PCM byte format (no bit inverted, even bit inverted, odd bit inverted or all bit inverted) and the presence or not of the extra bit.

◊ conference connection: the user specifies which channel to be connected to which conference with the attenuation or gain levels to be applied to the PCM signal coming in and/or sent out.

◊ transparent connection: the user specifies which channel to be connected in transparent mode (bypass mode) with the attenuation or gain levels to be applied to the PCM signal coming in and/or sent out.

◊ tone generation: the user specifies to which channel the tone must be sent out with the attenuation or gain levels and the tone sequence. The sequence is composed of maximum 4 pairs of frequency-duration for tone and maximum 32 pairs of frequency-duration for melody. The frequency range is 3.9Hz to 3938Hz and the duration range is from 32ms to 8610ms. The user can specify either all of the pairs or finish the sequence with the byte hex FF. The M34116 will loop the specified sequence endlessly or until the channel is disconnected. The melody could be either a sine or square wave (pin programmable).

◊ channel disconnection: the user specifies which channel to be disconnected. A disconnected channel can be reconnected only after a minimum of one frame time.

◊ overflow status. The user specifies which of the 4 banks of 8 conferences to be monitored and the M34116 will send the status byte at the read operation.

◊ channel status. The user specifies the channel number and the M34116 will send out the status bytes at the read operation. These bytes include: conference number or transparent mode or tone or no connection, input attenuation or gain levels, output attenuation or gain levels. If the channel is in the tone mode, the tone sequence of frequency and duration will also be sent out.

INSTRUCTION SET

OPERATING MODES

Two different operating mode istructions are available:

M116 Operating Mode:
Sending this operating mode instruction, the device functionality is the same as M116 and M116 instruction set is selected (refer to the following M116 instruction set for further details).

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	X	E	F1	F0	0	1	0	1

❖ E = 1 extra bit

❖ F1– F0 = 00 no bit inverted
01 even bit inverted
10 odd bit inverted
11 all bit inverted

Default values after reset:

E = 0 F1– F0 = 11 if MU Law
F1– F0 = 01 if A Law

M34116 Operating Mode:
Sending this operating mode instruction, the M34116 instruction set and functionality are selected

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	X	E	F1	F0	1	0	0	1

❖E = 1 extra bit

❖F1– F0 = 00 no bit inverted
01 even bit inverted
10 odd bit inverted
11 all bit inverted

Note:
Upon reset M116 instruction set is automatically selected. To switch from the M116 instruction set the above M34116 operating mode instruction is necessary. The operating mode instruction, when necessary, must be sent just after reset.

M34116 INSTRUCTION SET.

INSTRUCTION 1: M34116 CHANNEL CONNECTION IN CONFERENCE MODE
Five bytes are needed:

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	X	X	S	P4	P3	P2	P1	P0
0	1	0	0	X	X	X	Al4	Al3	Al2	Al1	Al0
0	1	0	0	X	X	X	AO4	AO3	AO2	AO1	AO0
0	1	0	0	X	PT	C5	C4	C3	C2	C1	C0
0	1	1	0	X	X	X	X	0	1	1	1

❖ S: Start bit

❖ Al4–Al0: Input attenuation or gain (±15dB)
Al4 = 1 gain
Al4 = 0 attenuation
Al3–Al0 value in dB (0–15)

❖ Ol4–AO0: output attenuation or gain (±15dB)
AO4 = 1 gain
AO4 = 0 attenuation
AO3–AO0 value in dB (0–15)

❖ PT: Phase toggle conference
❖ P4–P0: Conference number (1–29)
❖ C5–C0: Channel number (0–63)

When S = 1 the conference register is cleared.
S = 1 can be used only when connecting the first channel to a new conference.

When PT = 1 the sign of the PCM samples is changed before they are put in conference. This corresponds to a phase shift of 180° and may be used to reduce the electrical echo.

Note: Unspecified Data Bus can be either 0's or 1's

M34116 INSTRUCTION SET (continued)

INSTRUCTION 2: M34116 CHANNEL CONNECTION IN TRANSPARENT MODE
Four bytes are needed:

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	X	X	X	AI4	AI3	AI2	AI1	AI0
0	1	0	0	X	X	X	AO4	AO3	AO2	AO1	AO0
0	1	0	0	X	X	C5	C4	C3	C2	C1	C0
0	1	1	0	X	X	X	X	0	0	1	1

- ❖ AI4–AI0: Input attenuation or gain (±15dB)
  - AI4 = 1 gain
  - AI4 = 0 attenuation
  - AI3–AI0 value in dB (0–15)
- ❖ AO4–AO0: output attenuation or gain (±15dB)
  - AO4 = 1 gain
  - AO4 = 0 attenuation
  - AO3–AO0 value in dB (0–15)
- ❖ C5–C0: Channel number (0–63)

INSTRUCTION 3: M34116 CHANNEL DISCONNECTION
This instruction is necessary to disconnect a party from a conference, to end a transparent mode connection or to end a tone generation.
Two bytes are needed (same format as M116):

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	X	X	C5	C4	C3	C2	C1	C0
0	1	1	0	X	X	X	X	1	1	1	1

C5–C0: Channel number (0–63)

One time frame must exist between disconnection and connection of the same channel.

INSTRUCTION 4: M34116 OVERFLOW INFORMATION
Single byte instruction:

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	X	X	B1	B0	1	0	1	0

❖ B1–B0: Bank Selection (0–3)

Conference overflow information is sent out, after this instruction, in the data bus (D7–D0) when $\overline{RD}$ goes low according to the Bank selection value:

Control Signal				Bank Selection		Conference Number							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	B1	B0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	7	6	5	4	3	2	1	X
0	0	0	1	0	1	15	14	13	12	11	10	9	8
0	0	0	1	1	0	23	22	21	20	19	18	17	16
0	0	0	1	1	1	X	X	29	28	27	26	25	24

M34116 INSTRUCTION SET (continued)
INSTRUCTION 5: M34116 TONE GENERATION

Up to 7 Tone and 1 Melody channels may be active simultaneously. The instruction format for Tone and Melody is the same. For each Tone channel from 1 up to 4 couples of Step/Time may be specified while for the Melody channel from 1 up to 32 couples of Step/Time may be specified.
Note:
The Melody channel can be channel 0 or 8 or 16 or 24 etc. according to the following formula:

Melody channel number = 0 + 8 x n (n = 0, 1, 2, 3, 4, 5, 6, 7)

The Tone channel assignment follows the same rule:

Tone 1 channel number = 1 + 8 x n (n = 0, 1, 2, 3, 4, 5, 6, 7)
Tone 2 channel number = 2 + 8 x n (n = 0, 1, 2, 3, 4, 5, 6, 7)
. . . . . .
Tone 7 channel number = 7 + 8 x n (n = 0, 1, 2, 3, 4, 5, 6, 7)

This means that, selecting the tone 1 on the channel 9 (or and other one of its series), the channels 1, 17, 25.... can not be used for tones (or melody). The same is occuring for the tones 2...7 or the melody.

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0				AO4	AO3	AO2	AO1	AO0
0	1	0	0				C4	C3	C2	C1	C0
0	1	1	0					1	1	0	0
0	1	0	0	S17	S16	S15	S14	S13	S12	S11	S10
0	1	0	0	T17	T16	T15	T14	T13	T12	T11	T10
0	1	0	0	S27	S26	S25	S24	S23	S22	S21	S20
0	1	0	0	T27	T26	T25	T24	T23	T22	T21	T20
:	:	:	:	:	:	:	:	:	:	:	:

optional end code:

0	1	0	0	1	1	1	1	1	1	1	1

opcode:

0	1	1	0					1	1	0	0

❖ AO4–AO0: Output attenuation or gain (±15dB) AO4 = 1 gain, AO4 = 0 attenuation,
AO3–AO0 value in dB (0–15)
0dB attenuation or gain correspond to -6dBm0 level.

❖ C5–C0: Channel number (0–63)

❖ Sn7–Sn0: Frequency Step for the n–th note in the tone sequence (n = 1–4 for tone n = 1–32 for melody). Step is a compressed coding of the frequency value. Given a frequency value f the value of S7–S0 can be calculated as follow:

1) calculate the linear step SL = round $\left(f \times \frac{32}{125} \right)$

2) apply the following table to get S7–S0 value from SL value (see also Appendix 1A and 1B).

S7	S6	Linear Step SL value (10 bit)										(SL decimal)	STEP (Hz)
0	0	0	0	0	0	S5	S4	S3	S2	S1	S0	(1→64) **(*)**	3.9
0	0	0	0	0	1	S5	S4	S3	S2	S1	S0	(65–>127) **(**)**	3.9
0	1	0	0	1	S5	S4	S3	S2	S1	S0	0	(128–>254)	7.8
1	0	0	1	S5	S4	S3	S2	S1	S0	0	0	(256–>508)	15.6
1	1	1	S5	S4	S3	S2	S1	S0	0	0	0	(512–>1008)	31.2

(*) For tone 7 only; **(**)** For melody and tone 1-6

Note: to obtain a Pause (Silence) –> S7–S0 must be all 0's

❖ End code: if Less than 4 couples of Step/Time for tone or less than 32 for melody are to be specified then after the last couple of Step/Time a Step of all 1's (optional end code) must be sent before the opcode. Otherwise it must be skipped.

❖ Tn7–Tn0: Specify the duration of the n'th note or pause. The time increment is 32ms. To get T7–T0 value, divide the wanted duration in ms by 32 and round to integer.

Note: The minimum time between rising edges of successive $\overline{WR}$ for tone generation instruction is 4ck periods (6ck periods if EC = 1).

M34116 INSTRUCTION SET (continued)

INSTRUCTION 6: M34116 STATUS
The Status instruction can be used to read the contents of the instruction register and of the tone and melody registers.

Two byte are needed:

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0			C5	C4	C3	C2	C1	C0
0	1	1	0					0	1	1	0

❖ C5–C0: Channel number (0–63)

After sending this instruction a variable number of Read can be sent depending on the type of operation that performs the channel (conference, transparent, tone, or melody). The first 3 Read, common to all type of operation, will send on the Data Bus the following data relative to the channel (C5–C0):

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	IT	PT		P4	P3	P2	P1	P0
0	0	0	1				AI4	AI3	AI2	AI1	AI0
0	0	0	1				AO4	AO3	AO2	AO1	AO0

Note:
P4–P0 = 0 means that the channel is disconnected so any following data read is meaningless.
P4–P0 = 1 to 29 is the conference number.
P4–P0 = 30 means that the channel operation is Tone or Melody.
P4–P0 = 31 means that the channel operation is transparent connection.

If the channel operation is Tone or Melody (P4 – P0 = 30) then the subsequent Read will send on the Data Bus the couples of Step/Time:

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	S17	S16	S15	S14	S13	S12	S11	S10
0	0	0	1	T17	T16	T15	T14	T13	T12	T11	T10
0	0	0	1	S27	S26	S25	S24	S23	S22	S21	S20
0	0	0	1	T27	T26	T25	T24	T23	T22	T21	T20
:	:	:	:	:	:	:	:	:	:	:	:

Notes:
–Tone and Melody status reading ends if an all 1's Step value is found, otherwise the reading is cyclic.
–The minimum time from the rising edge of the $\overline{WR}$ (with opcode) to the falling edge of first $\overline{RD}$ is 4clock periods (6clock periods if E = 1) unless the selected channel has been disconnected. In this case, one time frame must exist between the disconnect command and the read status command. The RD period is minimum 4clock periods (6clock periods if E = 1).
– for both modes (M34116 and M116) the minimum time between two successive rising edges of the WR with opcode (C/D = 1) is 4clock periods (6clock periods if E = 1).
E: Extra bit indication in "Operating mode" instruction.

M116 INSTRUCTION SET

INSTRUCTION 1: CHANNEL CONNECTION IN CONFERENCE MODE

Three byte are needed:

1)The first byte contains the conference number (bits D0–D3) and the Start bit S (bit D4). When S = 1, all registers of the conference will be cleared. S = 1 is only required in the instruction 1 set of the first channel connected to a new conference.

2)The second byte contains in the bits (D0–D4) the number of the channel to be connected and the Insert Tone Enable bit IT (D5). When bit IT = 1 all the channels belonging to that conference are enabled using insert tone function if it's active (TD = 1).

3) The third byte contains information about the attenuation level to be applied to that channel and the opcode (0111).

Instruction 1 Format

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	X	X	X	S	P3	P2	P1	P0
0	1	0	0	X	X	IT	C4	C3	C2	C1	C0
0	1	1	0	A1	A0	X	X	0	1	1	1

S: Conference Start bit
P3–P0: Conference number (1–10)
IT: Insertion Tone function enable (IT = 1)
C4–C0: Channel number (0–31)
A1–A0: Channel attenuation
00 = – 0dB
01 = – 3dB
10 = – 6dB

INSTRUCTION 2: CHANNEL CONNECTION IN TRANSPARENT MODE

Two bytes are needed:

1) The first byte contains the number of the channel.

2) The second byte contains information about the attenuation level to be applied to that channel and the opcode (0011).

PCM data of this channel is not added to any conference and it is transferred to the PCM output. It is not affected by the tone control pins.

Instruction 2 Format

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	X	X	X	C4	C3	C2	C1	C0
0	1	1	0	A1	A0	X	X	0	0	1	1

INSTRUCTION 3: CHANNEL DISCONNECTION

Two bytes are needed:

1) The first word contains the number of the channel to be disconnected.
2) The second word contains the opcode (1111).
One time frame must exist between disconnection and connection of the same channel.

Instruction 3 Format

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	X	X	X	C4	C3	C2	C1	C0
0	1	1	0	X	X	X	X	1	1	1	1

M116 INSTRUCTION SET (continued)

INSTRUCTION 4: OVERFLOW INFORMATION

Two bytes are needed to know the status of all 10 conferences: C/$\overline{D}$ = 0 reads the first byte (first 8 conferences) and C/D = 1 reads the second byte (the last 2 conferences). A conference is in overflow when the corresponding bit is high.

Instruction 4 Format

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1
0	0	1	1	X	X	X	X	X	X	CF10	CF9

CF10 – CF1: Conference in overflow when high.
nb: as long as RD remains low, the overflow status of the conference selected by C/$\overline{D}$ can be monitored in real time.

INSTRUCTION 5: OPERATING MODE

The single byte needed contains the Extra bit (D6), the format bits F1–F0 (D5–D4) and the opcode (0101).
The E bit must be E = 1 when the PCM frame contains a number of bit multiple of eight plus on bit (ex. PCM frame at 1544Kbit/s). Normally E = 0. The bits F1–F0 select the kinds of PCM format byte according table 1. After Reset the default values corresponds to F1 = 0, F0 = 1 if A–law is selected and F1 = 1, F0 = 1 if Mu–law is selected. All channels must be disconnected when the Operating Mode Instruction is sent. They must remain disconnected for at least two time frames after the instruction was sent.
We recommende to use this instruction right after the RESET (see pin $\overline{RESET}$ decription).

Instruction 5 Format

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	X	E	F1	F0	0	1	0	1

E: Extra bit insertion (active when E = 1)
F1 – F0: PCM byte Format selection (see also table 1)
00 = no bit inverted
01 = even bit (B0–B2–B4–B6) inverted
10 = odd bit (B1–B3–B5) inverted
11 = all bit (B0–B1–B2–B3–B4–B5–B6) inverted

INSTRUCTION 6: STATUS

Three bytes are needed:

1) The first byte contains the number of the channel;
2) The second byte contains the opcode (0110);
3) By a reding cycle you extract from the third byte the information about the operating mode of the channel (no connection or transparent mode or number of the conference, bits D4–D7); the attenuation (D2–D3) and noise suppression values (D0–D1) eventually inserted.
This reading cycle must be executed at least one frame after the end of the opcode writing cycle.

Instruction 6 Format

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	X	X	X	C4	C3	C2	C1	C0
0	1	1	0	X	X	X	X	0	1	1	0
0	0	1	1	P3	P2	P1	P0	A1	A0	T1	T0

P3–P0: channel mode operation information
0000 = no connection
1111 = transparent mode
1010 – 0001 = conference mode

P3–P0 give the number of the conferenc

nb: the instruction 6 enables the dat bus to read the status until reset by C/D = 0 and WR = 1.

Table 1 : PCM Byte Format. B7 (sign–bit) is the MSB and B0 is the LSB. F1–F0 corresponds to D5–D4 in the byte of the Operating Mode Instruction (instruction 5).

F1	F0		B7	B6	B5	B4	B3	B2	B1	B0
0	0	+FULL SCALE	1	1	1	1	1	1	1	1
			1	0	0	0	0	0	0	0
		MIN LEVELS	0	0	0	0	0	0	0	0
		–FULL SCALE	0	1	1	1	1	1	1	1
0	0	+FULL SCALE	1	0	1	0	1	0	1	0
			1	1	0	1	0	1	0	1
		MIN LEVELS	0	1	0	1	0	1	0	1
		–FULL SCALE	0	0	1	0	1	0	1	0
1	0	+FULL SCALE	1	1	0	1	0	0	0	0
			1	0	1	0	1	1	1	1
		MIN LEVELS	0	0	1	0	1	1	1	1
		–FULL SCALE	0	1	0	1	0	0	0	0

Figure 11: Overflow Control with µP Interactive Procedure

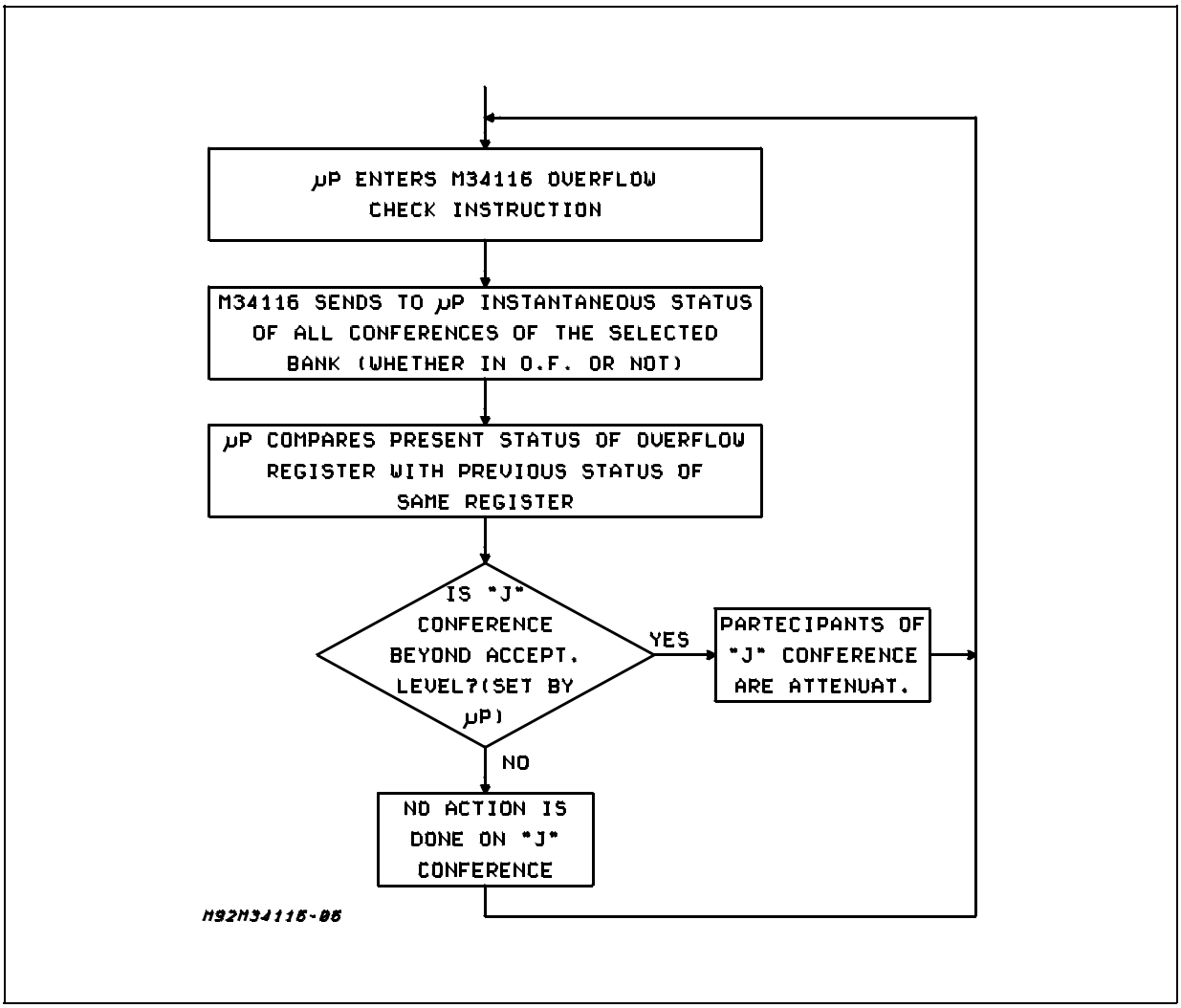
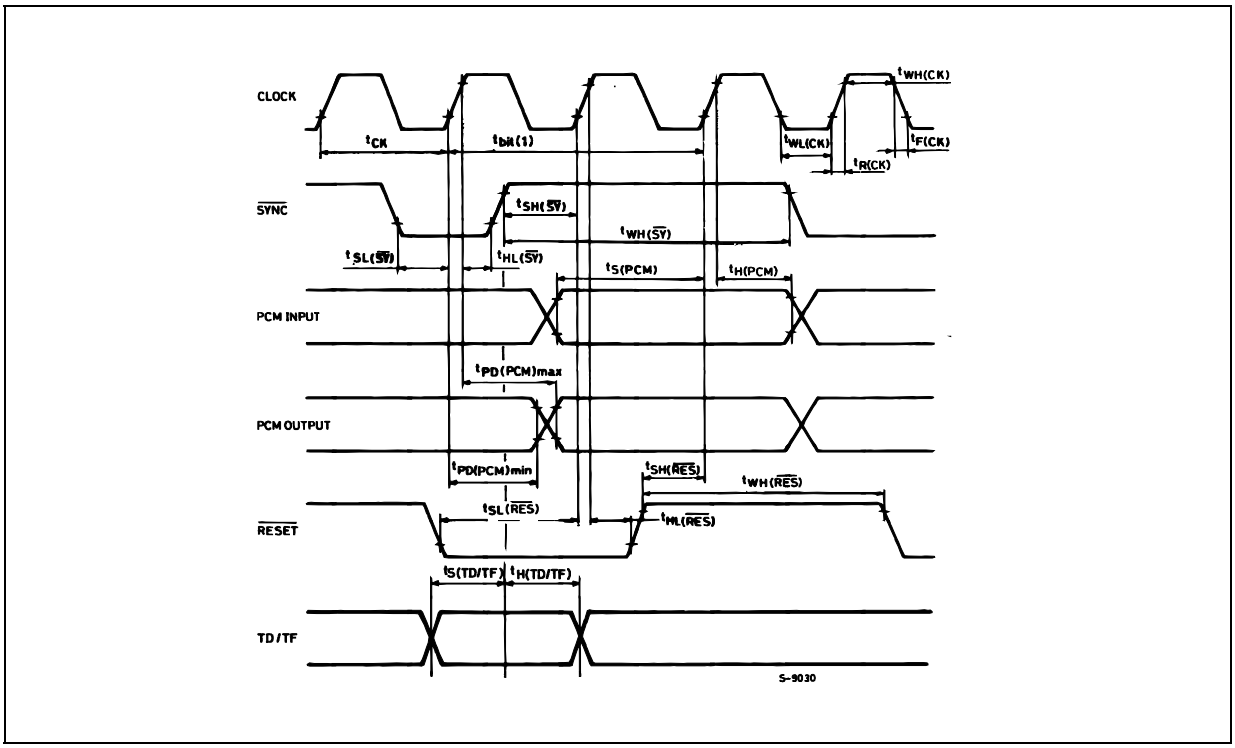


Figure 12: $\overline{\text{SYNC}}$, PCM I/O, $\overline{\text{RESET}}$, TD/TF Timings



(1) t_{bit} corresponds to bit 0, channel 0 or Extra Bit.

Figure 13: WRITE Operating Timing.

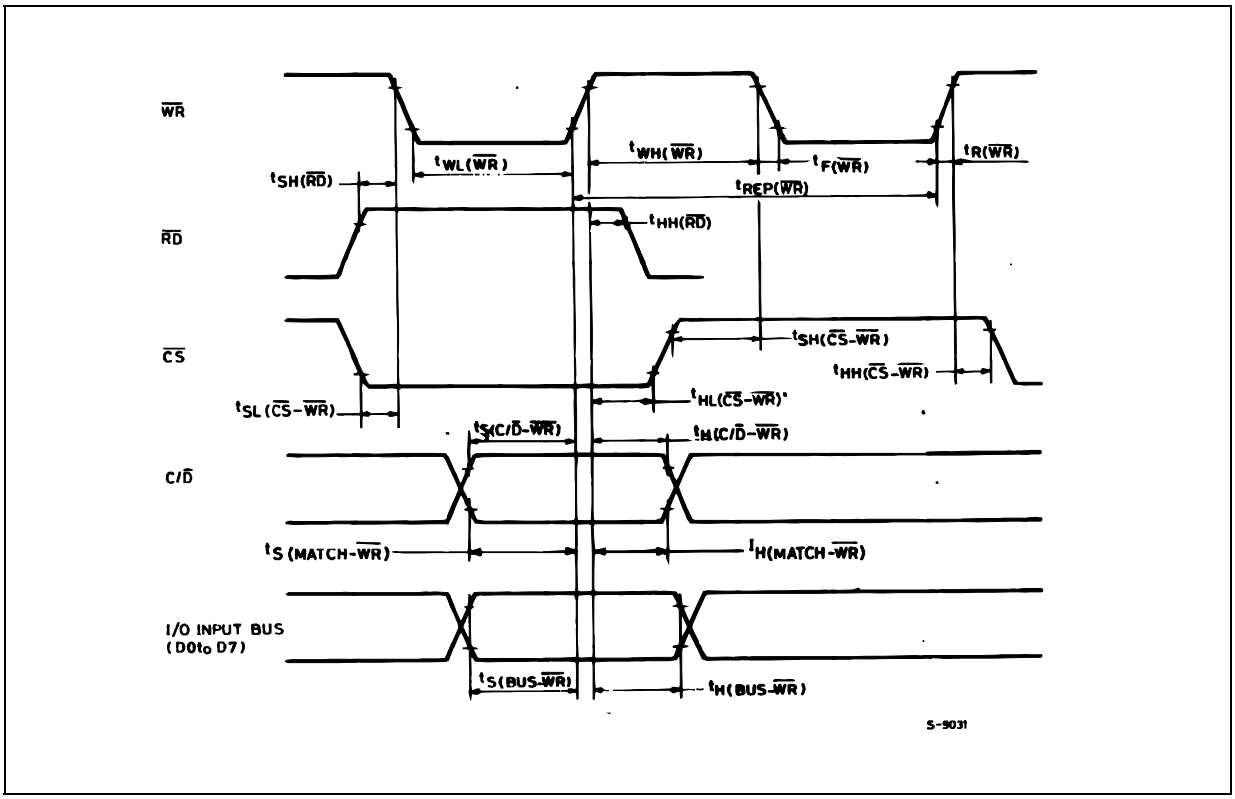


Figure 14: READ Operating Timing.

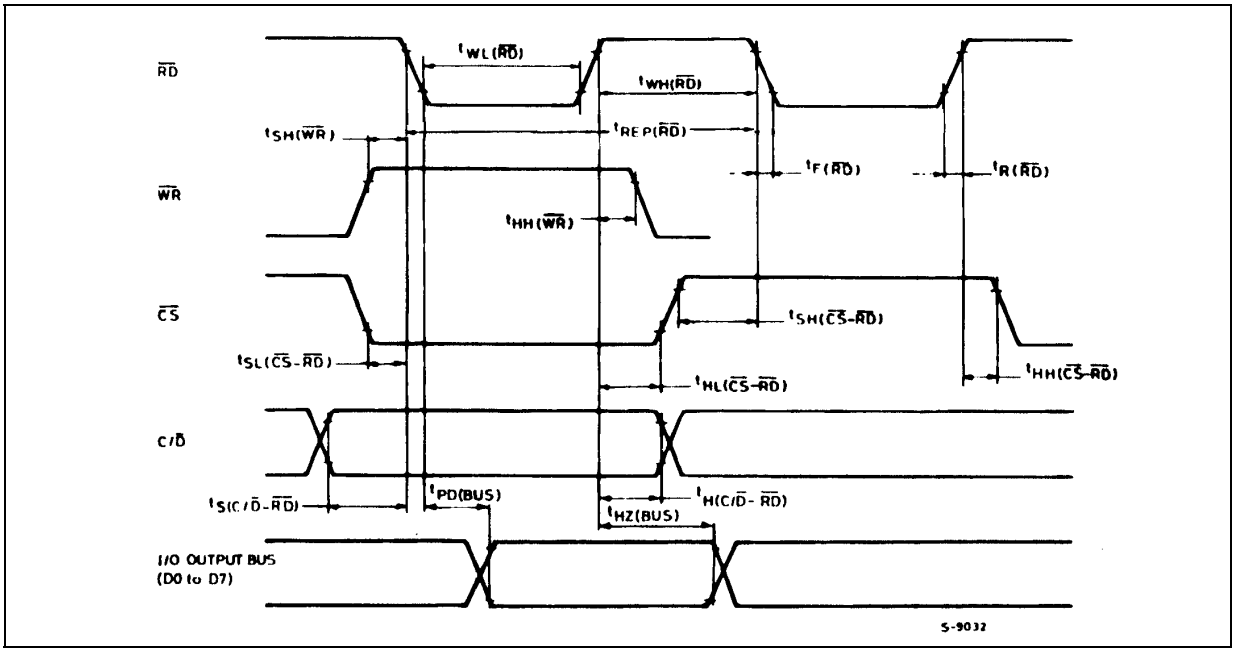


Figure 15: RC (External Clock) and $\overline{OS}$ (Overflow Signalling) Timings.

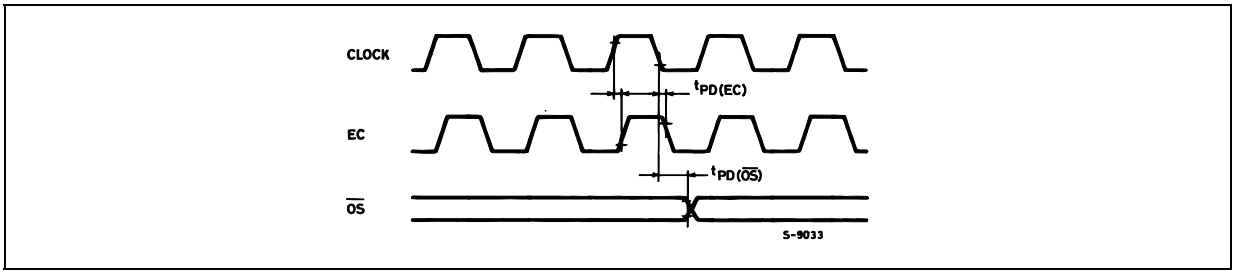


Figure 16: EC Timing with Extra Bit Operating Mode Insert.

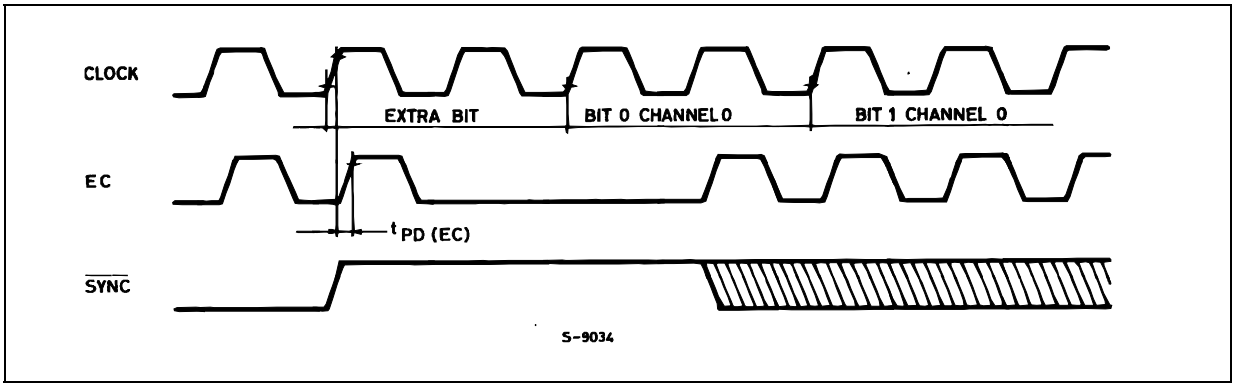
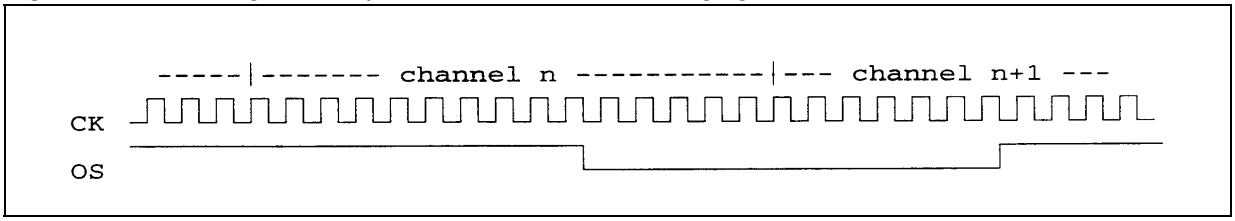


Figure 17: $\overline{OS}$ Timing with Output PCM Channel n+1 belonging to a Conference in Overflow.



APPENDIX 1A - Correspondance between S7-S0 values (HEX) and synthetized frequency for melody and tone 1-6:

00	SILENCE	40	500.00	80	1000.00	C0	2000.00
01	253.91	41	507.81	81	1015.62	C1	2031.25
02	257.81	42	515.62	82	1031.25	C2	2062.50
03	261.72	43	523.44	83	1046.88	C3	2093.75
04	265.62	44	531.25	84	1062.50	C4	2125.00
05	269.53	45	539.06	85	1078.12	C5	2156.25
06	273.44	46	546.88	86	1093.75	C6	2187.50
07	277.34	47	554.69	87	1109.38	C7	2218.75
08	281.25	48	562.50	88	1125.00	C8	2250.00
09	285.16	49	570.31	89	1140.62	C9	2281.25
0A	289.06	4A	578.12	8A	1156.25	CA	2312.50
0B	292.97	4B	585.94	8B	1171.88	CB	2343.75
0C	296.88	4C	593.75	8C	1187.50	CC	2375.00
0D	300.78	4D	601.56	8D	1203.12	CD	2406.25
0E	304.69	4E	609.38	8E	1218.75	CE	2437.50
0F	308.59	4F	617.19	8F	1234.38	CF	2468.75
10	312.50	50	625.00	90	1250.00	D0	2500.00
11	316.41	51	632.81	91	1265.62	D1	2531.25
12	320.31	52	640.62	92	1281.25	D2	2562.50
13	324.22	53	648.44	93	1296.88	D3	2593.75
14	328.12	54	656.25	94	1312.50	D4	2625.00
15	332.03	55	664.06	95	1328.12	D5	2656.25
16	335.94	56	671.88	96	1343.75	D6	2687.50
17	339.84	57	679.69	97	1359.38	D7	2718.75
18	343.75	58	687.50	98	1375.00	D8	2750.00
19	347.66	59	695.31	99	1390.62	D9	2781.25
1A	351.56	5A	703.12	9A	1406.25	DA	2812.50
1B	355.47	5B	710.94	9B	1421.88	DB	2843.75
1C	359.38	5C	718.75	9C	1437.50	DC	2875.00
1D	363.28	5D	726.56	9D	1453.12	DD	2906.25
1E	367.19	5E	734.38	9E	1468.75	DE	2937.50
1F	371.09	5F	742.19	9F	1484.38	DF	2968.75
20	375.00	60	750.00	A0	1500.00	E0	3000.00
21	378.91	61	757.81	A1	1515.62	E1	3031.25
22	382.81	62	765.62	A2	1531.25	E2	3062.50
23	386.72	63	773.44	A3	1546.88	E3	3093.75
24	390.62	64	781.25	A4	1562.50	E4	3125.00
25	394.53	65	789.06	A5	1578.12	E5	3156.25
26	398.44	66	796.88	A6	1593.75	E6	3187.50
27	402.34	67	804.69	A7	1609.38	E7	3218.75
28	406.25	68	812.50	A8	1625.00	E8	3250.00
29	410.16	69	820.31	A9	1640.62	E9	3281.25
2A	414.06	6A	828.12	AA	1656.25	EA	3312.50
2B	417.97	6B	835.94	AB	1671.88	EB	3343.75
2C	421.88	6C	843.75	AC	1687.50	EC	3375.00
2D	425.78	6D	851.56	AD	1703.12	ED	3406.25
2E	429.69	6E	859.38	AE	1718.75	EE	3437.50
2F	433.59	6F	867.19	AF	1734.38	EF	3468.75
30	437.50	70	875.00	B0	1750.00	F0	3500.00
31	441.41	71	882.81	B1	1765.62	F1	3531.25
32	445.31	72	890.62	B2	1781.25	F2	3562.50
33	449.22	73	898.44	B3	1796.88	F3	3593.75
34	453.12	74	906.25	B4	1812.50	F4	3625.00
35	457.03	75	914.06	B5	1828.12	F5	3656.25
36	460.94	76	921.88	B6	1843.75	F6	3687.50
37	464.84	77	929.69	B7	1859.38	F7	3718.75
38	468.75	78	937.50	B8	1875.00	F8	3750.00
39	472.66	79	945.31	B9	1890.62	F9	3781.25
3A	476.56	7A	953.12	BA	1906.25	FA	3812.50
3B	480.47	7B	960.94	BB	1921.88	FB	3843.75
3C	484.38	7C	968.75	BC	1937.50	FC	3875.00
3D	488.28	7D	976.56	BD	1953.12	FD	3906.25
3E	492.19	7E	984.38	BE	1968.75	FE	3937.50
3F	496.09	7F	992.19	BF	1984.38	FF	3968.75

APPENDIX 1B - Correspondence between S7-S0 values (HEX) and synthetized frequency for tone 7:

0	SILENCE	40	500.00	80	1000.00	c0	2000.00
1	3.91	41	507.81	81	1015.62	c1	2031.25
2	7.81	42	515.62	82	1031.25	c2	2062.50
3	11.72	43	523.44	83	1046.88	c3	2093.75
4	15.62	44	531.25	84	1062.50	c4	2125.00
5	19.53	45	539.06	85	1078.12	c5	2156.25
6	23.44	46	546.88	86	1093.75	c6	2187.50
7	27.34	47	554.69	87	1109.38	c7	2218.75
8	31.25	48	562.50	88	1125.00	c8	2250.00
9	35.16	49	570.31	89	1140.62	c9	2281.25
a	39.06	4a	578.12	8a	1156.25	ca	2312.50
b	42.97	4b	585.94	8b	1171.88	cb	2343.75
c	46.88	4c	593.75	8c	1187.50	cc	2375.00
d	50.78	4d	601.56	8d	1203.12	cd	2406.25
e	54.69	4e	609.38	8e	1218.75	ce	2437.50
f	58.59	4f	617.19	8f	1234.38	cf	2468.75
10	62.50	50	625.00	90	1250.00	d0	2500.00
11	66.41	51	632.81	91	1265.62	d1	2531.25
12	70.31	52	640.62	92	1281.25	d2	2562.50
13	74.22	53	648.44	93	1296.88	d3	2593.75
14	78.12	54	656.25	94	1312.50	d4	2625.00
15	82.03	55	664.06	95	1328.12	d5	2656.25
16	85.94	56	671.88	96	1343.75	d6	2687.50
17	89.84	57	679.69	97	1359.38	d7	2718.75
18	93.75	58	687.50	98	1375.00	d8	2750.00
19	97.66	59	695.31	99	1390.62	d9	2781.25
1a	101.56	5a	703.12	9a	1406.25	da	2812.50
1b	105.47	5b	710.94	9b	1421.88	db	2843.75
1c	109.38	5c	718.75	9c	1437.50	dc	2875.00
1d	113.28	5d	726.56	9d	1453.12	dd	2906.25
1e	117.19	5e	734.38	9e	1468.75	de	2937.50
1f	121.09	5f	742.19	9f	1484.38	df	2968.75
20	125.00	60	750.00	a0	1500.00	e0	3000.00
21	128.91	61	757.81	a1	1515.62	e1	3031.25
22	132.81	62	765.62	a2	1531.25	e2	3062.50
23	136.72	63	773.44	a3	1546.88	e3	3093.75
24	140.62	64	781.25	a4	1562.50	e4	3125.00
25	144.53	65	789.06	a5	1578.12	e5	3156.25
26	148.44	66	796.88	a6	1593.75	e6	3187.50
27	152.34	67	804.69	a7	1609.38	e7	3218.75
28	156.25	68	812.50	a8	1625.00	e8	3250.00
29	160.16	69	820.31	a9	1640.62	e9	3281.25
2a	164.06	6a	828.12	aa	1656.25	ea	3312.50
2b	167.97	6b	835.94	ab	1671.88	eb	3343.75
2c	171.88	6c	843.75	ac	1687.50	ec	3375.00
2d	175.78	6d	851.56	ad	1703.12	ed	3406.25
2e	179.69	6e	859.38	ae	1718.75	ee	3437.50
2f	183.59	6f	867.19	af	1734.38	ef	3468.75
30	187.50	70	875.00	b0	1750.00	f0	3500.00
31	191.41	71	882.81	b1	1765.62	f1	3531.25
32	195.31	72	890.62	b2	1781.25	f2	3562.50
33	199.22	73	898.44	b3	1796.88	f3	3593.75
34	203.12	74	906.25	b4	1812.50	f4	3625.00
35	207.03	75	914.06	b5	1828.12	f5	3656.25
36	210.94	76	921.88	b6	1843.75	f6	3687.50
37	214.84	77	929.69	b7	1859.38	f7	3718.75
38	218.75	78	937.50	b8	1875.00	f8	3750.00
39	222.66	79	945.31	b9	1890.62	f9	3781.25
3a	226.56	7a	953.12	ba	1906.25	fa	3812.50
3b	230.47	7b	960.94	bb	1921.88	fb	3843.75
3c	234.38	7c	968.75	bc	1937.50	fc	3875.00
3d	238.28	7d	976.56	bd	1953.12	fd	3906.25
3e	242.19	7e	984.38	be	1968.75	fe	3937.50
3f	246.09	7f	992.19	bf	1984.38	ff	3968.75

APPENDIX 2

TONE GENERATION PROGRAMMING

Example 1:

f = 425Hz

Duration 200ms ON, 200ms OFF, 600ms ON, 1000ms OFF

Attenuation 10dB

Channel #0.

Programming sequence:

Control Signal				Data
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7 . . . . D0
0	1	0	0	0AH
0	1	0	0	00H
0	1	1	0	0CH
0	1	0	0	2DH
0	1	0	0	06H
0	1	0	0	00H
0	1	0	0	06H
0	1	0	0	2DH
0	1	0	0	12H
0	1	0	0	00H
0	1	0	0	1FH
0	1	1	0	0CH

Example 2:

f = 400Hz

Duration: 375ms ON, 375ms OFF

Attenuation 5dB

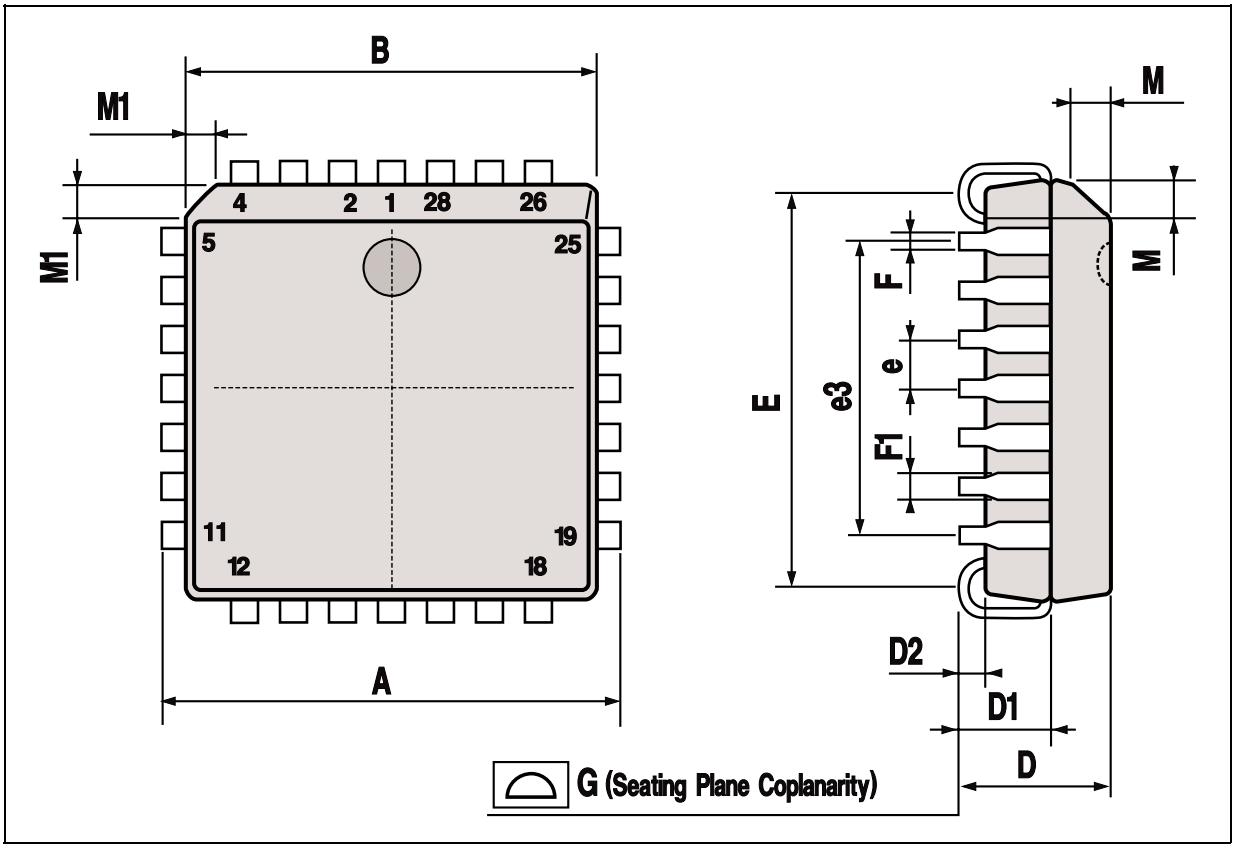
Channel #3

Programming sequence:

Control Signal				Data
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7 . . . . D0
0	1	0	0	05H
0	1	0	0	03H
0	1	1	0	0CH
0	1	0	0	26H
0	1	0	0	0CH
0	1	0	0	00H
0	1	0	0	0CH
0	1	0	0	FFH
0	1	1	0	0CH

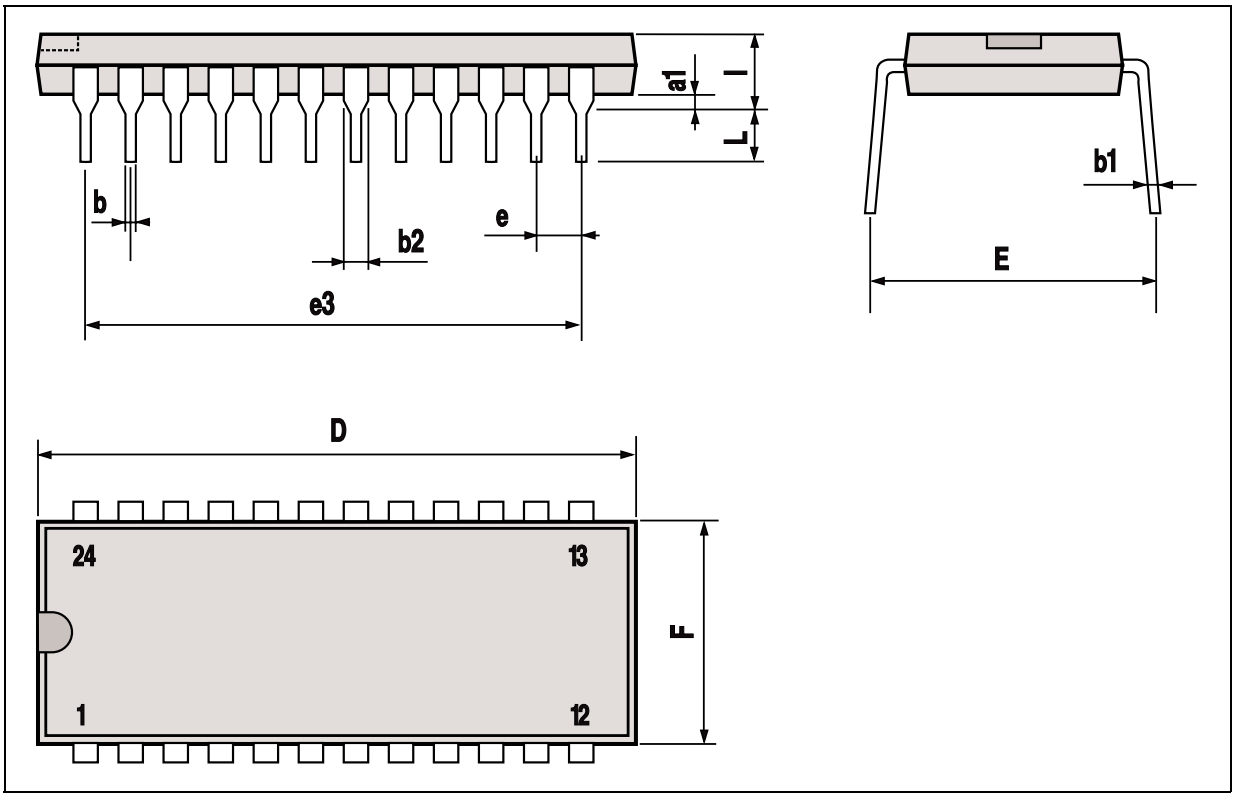
PLCC28 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	12.32		12.57	0.485		0.495
B	11.43		11.58	0.450		0.456
D	4.2		4.57	0.165		0.180
D1	2.29		3.04	0.090		0.120
D2	0.51			0.020		
E	9.91		10.92	0.390		0.430
e		1.27			0.050	
e3		7.62			0.300	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.24			0.049	
M1		1.143			0.045	



DIP24 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			32.2			1.268
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		27.94			1.100	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	



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