ISSUE 4 November 1990

Features

- Transparent coding and decoding of 0 to 8, 9.6 and 19.2 kbps data
- Coding compatible to PCM voice channels at 56/64 kbps in ST-BUS format
- Automatic line polarity detection and correction
- Loopback facility for test purposes
- Selectable data formats: RZ or NRZ
- Eight user selectable modes of operation
- Low power ISO-CMOS technology

Applications

- Transparent coder/decoder for synchronous and asynchronous data
- Data terminal (RS-232C, etc.) to ST-BUS interface
- Data switching on digital PBXs
- Channel banks/TDM multiplexers

Ordering Information

MT8950AC 24 Pin Ceramic DIP

0°C to 70°C

Description

The MT8950 is a coder/decoder which uses the Transition Encoded Modulation (TEM) technique for encoding/decoding low speed data to and from a 56/64 kbps channel (equivalent to PCM Voice). The coding and decoding scheme is transparent and can accept either synchronous or asynchronous data up to 8 kbps (inclusive); at 9.6 kbps and 19.2 kbps.

The MT8950 is fabricated in MITEL's ISO-CMOS technology.

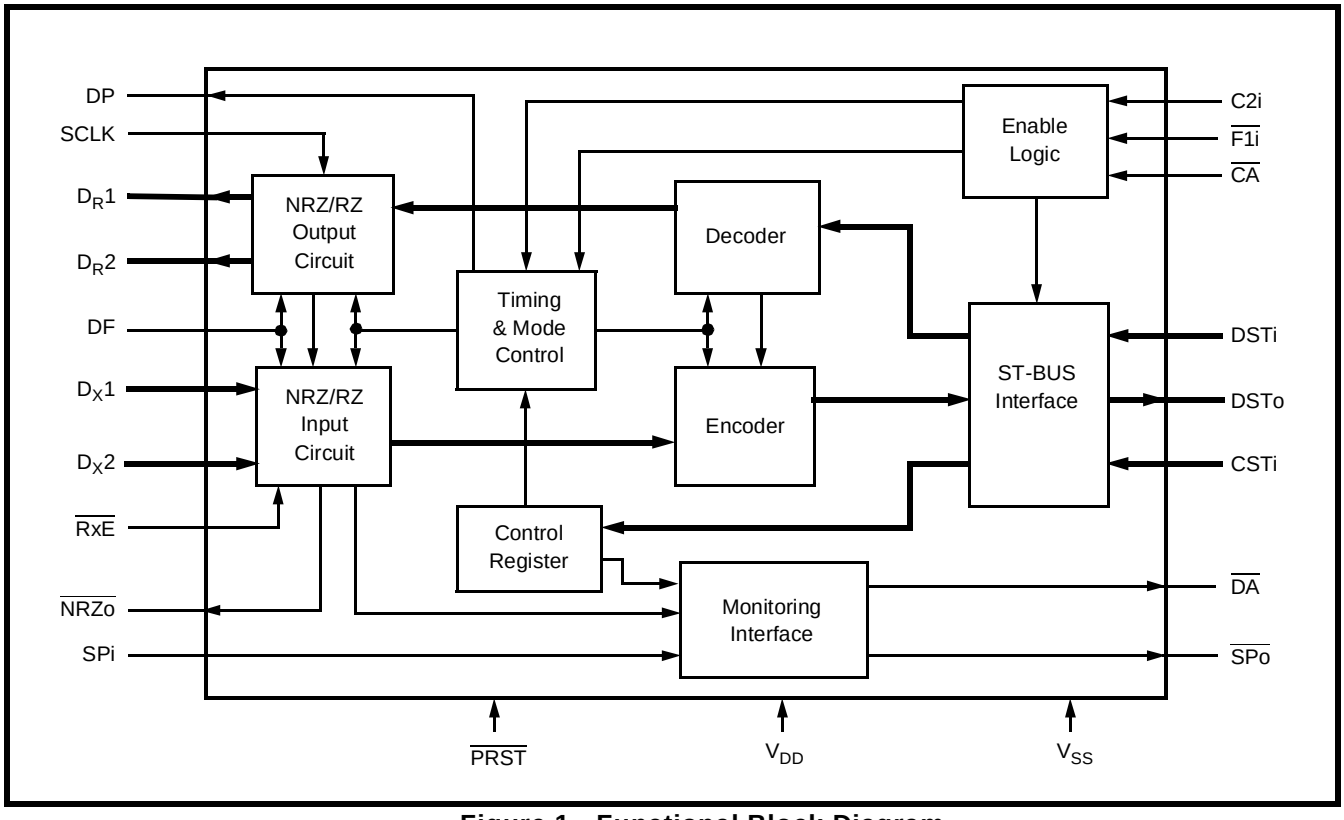


Figure 1 - Functional Block Diagram

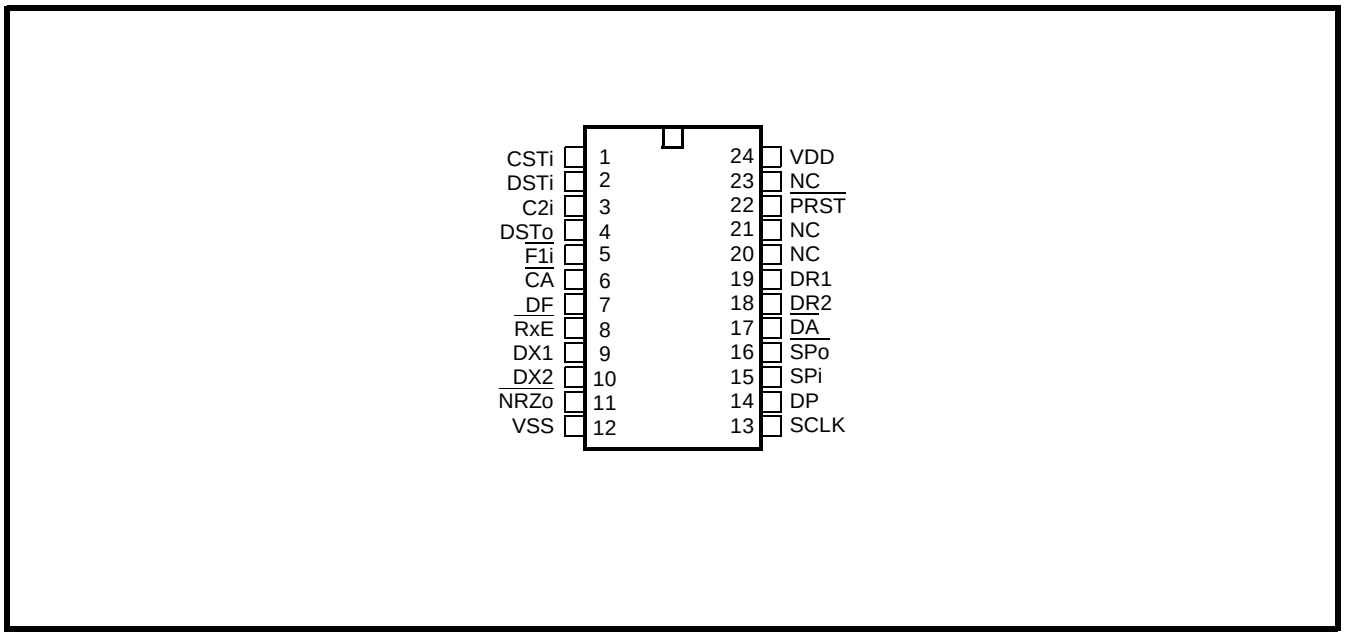


Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	CSTi	**Control ST-BUS In (TTL Input) -** This ST-BUS interface pin accepts a serial input stream which loads the Control Register. The mode of operation of the device, the bits in the Violation word, and, the resetting of Data Activity ($\overline{DA}$) and Scan Point output ($\overline{SPo}$) are controlled by this register. The contents of the register are updated once every ST-BUS frame when the interface is enabled.
2	DSTi	**Data ST-BUS In (TTL Input) -** Accepts the 8 bits of TEM Data when the ST-BUS interface is enabled.
3	C2i	**2.048 MHz Clock (TTL Input) -** This is the input for the 2.048 MHz clock.
4	DSTo	**ST-BUS Output (Three-State Output) -** This is the 2.048 Mbps serial output for theTEM encoded word. It is enabled when both $\overline{F1i}$ and $\overline{CA}$ are low.
5	$\overline{F1i}$	**Framing Type 1 Input (TTL Input) -** This active low input, in conjunction with $\overline{CA}$, enables the ST-BUS interface (DSTi, DSTo and CSTi). It is internally sampled on every positive edge of the C2i clock and provides frame synchronization.
6	$\overline{CA}$	**Control Address (TTL Input) -** This active low input (in conjunction with $\overline{F1i}$) enables the ST-BUS interface.
7	DF	**Data Format Select (CMOS Input) -** When HIGH, the Data Codec accepts and delivers the data in unipolar Return to Zero (RZ) format. When LOW, the data format is unipolar NRZ.
8	$\overline{RxE}$	**Received Energy Signal (Schmitt Input) -** When $\overline{RxE}$ goes LOW it establishes the polarity of the input pins D_X1 and D_X2 in the RZ mode. The input which received the last pulse before $\overline{RxE}$ goes LOW is established as the unipolar MARK input. $\overline{RxE}$ also enables the operation of $\overline{DA}$ and $\overline{SPo}$ outputs the loopback modes (Modes 4, 5 and 6) of the codec, $\overline{RxE}$ is forced to the LOW state internally independent of the pin condition. $\overline{RxE}$ should be exerted LOW for the duration of a data call.
9	D_X1	**Data Transmit 1 (Schmitt Input) -** If DF= LOW, accepts data in the NRZ format. (HIGH = MARK, LOW = SPACE). If DF=HIGH, accepts active low unipolar pulses representing the digital data in the RZ format. MARK or SPACE polarity is established by the $\overline{RxE}$ input.

Pin Description (continued)

Pin #	Name	Description
10	D_X2	**Data Transmit 2 (Schmitt Input)** - If DF = LOW, accepts data pulses which are encoded only if there is no activity on the D_X1 pin - the data format and restrictions on the use of this input is explained in the text. If DF= HIGH, accepts active low unipolar pulses representing the digital data in the RZ format. MARK or SPACE polarity is established by the $\overline{RxE}$ input.
11	$\overline{NRZo}$	**Non-Return to Zero Output (Open Drain Output) -** The incoming data, in the RZ format or the NRZ format , is internally converted to inverted NRZ and appears on this open drain output. This output in conjunction with the SPi input can be used for long space detection.
12	V_{SS}	**Ground (0 Volt).**
13	SCLK	**Secondary Clock (TTL Input) -** This is an external clock input that determines the timing of the Violation Word and the synchronization pulses. If these features are not to be utilized, this input can be tied to V_{SS}.
14	DP	**Drive Point Output (Totem-pole Output) -** This output is exerted high when the Control Register bits b7, b6 and b5 are set to 110 (decimal 6). The operation of the Codec is normal in every other respect.
15	SPi	**Uncommitted Scan Point Input (Voltage Comparator Input) -** A LOW to HIGH transition on this input causes $\overline{SPo}$ to be set LOW. This is used to detect a long SPACE condition in conjunction with $\overline{NRZo}$ (pin 11).
16	$\overline{SPo}$	**Uncommitted Scan Point Output (Totem-pole Output) -** This output is set LOW when the SPi input undergoes a LOW to HIGH transition. The $\overline{SPo}$ is reset by the presence of a logic "1" in bit b0 of Control Register. This function is active at all times except when $\overline{RxE}$ is false and during power reset conditions.
17	$\overline{DA}$	**Data Activity (Totem-pole Output) -** The NRZ/RZ input circuitry monitors the input signal (after polarity is established) and activates this output when it detects a SPACE on the input. This output is reset by the presence of a logic "1" in bit 1 of the Control Register. The $\overline{DA}$ function is active at all times except when $\overline{RxE}$ is false and during power reset conditions.
18	D_R2	**Data Receive 2 (Totem-pole Output) -** If DF = LOW (NRZ format), outputs the secondary data signal in the NRZ form as explained in the text. If DF = HIGH (RZ format), outputs unipolar, active high MARK pulses.
19	D_R1	**Data Receive 1 (Totem-pole Output)** - If DF = LOW (NRZ format) , outputs the NRZ data signal. (HIGH = MARK, LOW = SPACE) If DF = HIGH (RZ format), outputs unipolar, active low SPACE pulses.
20	NC	**No connection.**
21	NC	**No connection.**
22	$\overline{PRST}$	**Power Reset (CMOS Schmitt Input) -** A LOW level on this input evokes the power reset condition for the codec.
23	NC	**No connection.**
24	V_{DD}	**Positive Supply Voltage +5 volts ± 10% .**

Theory of Operation

The MT8950 is an encoder/decoder which operates on low baud rate data (up to 19.2 kbps) to convert it to the ST-BUS format. The data can subsequently be transparently switched or transmitted in a manner identical to PCM encoded voice. In this respect, the functional characteristics of the device are very similar to many industry standard voice codecs. Asynchronous and synchronous data from 0 to 8 kbps and at 9.6 kbps is accepted by the codec without any restrictions. Asynchronous data at 19.2 kbps should have at least two stop bits for the device to encode it properly. The data is encoded by the Codec into an eight bit word which occupies one 64 kbps channel on the ST-BUS. Conversely, it accepts an encoded 8 bit word from an incoming ST-BUS stream and regenerates the original digital signal. Mitel's ST-BUS is a synchronous time division multiplexed serial stream with a bit rate of 2048 kbps. In a telecommunications environment, it is generally divided into 32 channels made up of 8 bits each, with an effective bandwidth of 64 kbps per channel. These channels may carry data or PCM encoded voice.

Low Speed Data Format

The Data Codec can accept low speed data in either Non Return to Zero (NRZ) or Return to Zero (RZ) format. The NRZ format requires only one line to carry the data. This format is suitable for interfacing the data codec with RS-232 type terminals and microprocessor peripherals such as UARTS, ACIAs, etc. All signals have to be converted to TTL voltage levels before being input to the codec.

The RZ format requires two separate lines to represent the MARKs and SPACEs in the data as illustrated in Figure 4. This format is useful when the data terminal is located some distance from the codec and the data is to be transmitted over a line as a three level signal (a positive pulse for the beginning of MARKs, negative pulse for the beginning of SPACEs and zero level for no change in the signal). The three level signal is converted to its TTL-Compatible binary form as shown in Figure 4 before being applied to the codec. A pulse appears on one line of the input indicating the beginning of MARKs. This is followed by a pulse on the second line indicating the beginning of SPACEs. If two or more pulses appear consecutively on the same line before the second line of the pair receives or transmits another pulse, then these pulses can be considered to be violating the normal rule of the RZ format and are called "Violation Pulses". The data codec will accept these violations with the restriction that the time difference between a violation pulse and an actual data transition be at least 125µs. The violation pulses can be on the MARK or SPACE line. In a communications system, these violations can be used to carry other information when no data is being transmitted.

Data Rate Bits/Sec	0 - 8000	9600	19200
Asynchronous Restrictions	None	None	Minimum 2 Stop Bits
Synchronous Restrictions	None	None	None
Percentage Distortion†	±3.2	±3.8	±7.5

Table 1. Summary of Data Codec Capabilities.

† Refers to the maximum distortion in the bit period timing of the regenerated data. (Channel Bandwidth = 64kbps)

Percentage Distortion = $|T_{BO} - T_{BR}| / T_{BO} \times 100$

where T_{BO} = Original Data Bit Period
T_{BR} = Regenerated Data Bit Period

Encoding/Decoding Scheme

The Data Codec uses a Transition Encoded Modulation (TEM) technique to encode low speed data onto a 56 or 64 kbps equivalent PCM voice channel. This coding algorithm significantly reduces data bit distortion. The timing distortion in the regenerated data is summarized in Table 1. A simple sampling method for encoding the data would require a 256 kbps channel to obtain the same low distortion figures.

If the encoded information is to be transmitted over digital T1/DS1 trunks, the maximum percentage distortion in the regenerated data is effectively doubled. This is due to the fact that the least significant bit in specific channels on these trunks is used to transmit signalling information. Thus the bandwidth per channel is reduced to 56 kbps.

The encoder stage of the Data Codec observes data transitions in discrete timing windows which are 125µs wide. These timing frames are further divided into 32 timeslots of 3.906µs duration each (see Figure 3). The position of the first data transition, the total number of transitions, and, the time period between the transitions in this 125µs frame is encoded as an 8 bit word.

The first five bits (b0 to b4) indicate the position of the first data transition with respect to the 32 timeslots in the window. Bit 7 in the encoded word represents the absolute value of the data in the 31st timeslot. Bits 5 and 6 in conjunction with bit 7 are used to identify the total number of transitions and the time period between the transitions. Due to the fixed bit rate restrictions above 8 kbps, a maximum

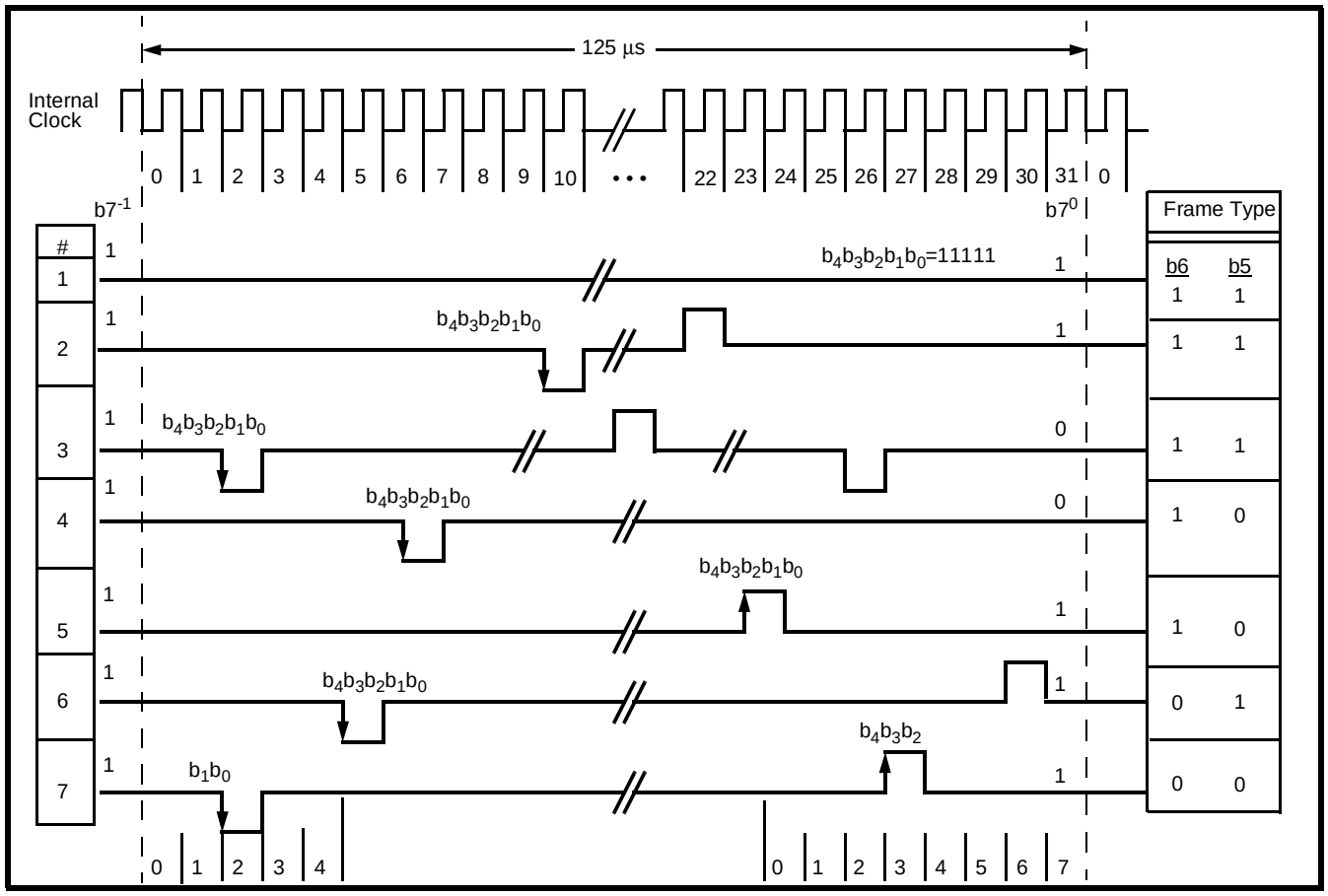


Figure 3 - TEM Coding Scheme

(Note: Waveforms shown are bipolar RZ equivalent of separate RZ/NRZ inputs)

#	Frame Description	Level† b7	Frame Type b6 b5	First Transition b4 b3 b2 b1 b0	Notes
1	No Pulse	1/0	1 1	1 1 1 1 1	
2	2 Data Pulses (T=52 µs)	1/0	1 1	X X X X X	X X X X X ≤ 10001 (17)
3	3 Data Pulses (T=52 µs)	1/0	1 1	X X X X X	X X X X X ≤ 00100 (4)
4	1 Data Pulse	1/0	1 0	X X X X X	X X X X X = 0 to 31
5	Violation Pulse	1/0	1 0	X X X X X	X X X X X = 0 to 31
6	2 Data Pulses (T=104 µs) (Timeslot 4 to 31)	1/0	0 1	X X X X X	X X X X X > 00011 (3)
7	2 Data Pulses (T=104 µs) (Timeslot 0 to 3)	1/0	0 0	Y Y Y X X	XX = 0 to 3 YYY = 0 to 7

Table 2. TEM Coding Summary

† Note: The Level bit (b7) indicates the level (HIGH or LOW) of the input data in timeslot 31 of the current frame.

of seven frames types are possible as shown in Figure 3. In frame type 7, the first five bits (b0 to b4) are used to represent two transitions instead of the normal first transition. Note that the data transitions in Figure 3 are shown as a three level signal. A positive transition indicates the beginning of one or more continuous MARKs and a negative transition indicates the beginning of one or more continuous SPACEs.

The decoder stage regenerates the original data from the 8 bit TEM word. The absolute values of the data signal in the present and previous frames as given by b7(n) and b7(n-1) are EX-ORed and the result in combination with the remaining bits of the TEM word is used to reproduce the original data with an accuracy of ± 3.906µs (see Table 2). Due to the data speed restriction above 8 kbps, the second and third transitions (if any) will be reproduced at

intervals which are multiples of 52µs (depending upon the input data baud rate).

Functional Description

The functional block diagram of the data codec is shown in Figure 1. The low speed data to be encoded is accepted by the NRZ/RZ input circuitry and relayed to the encoder. The 8 bit encoded word is transmitted within one channel time period on to the ST-BUS serial output stream. At the same time an 8 bit TEM word is loaded into the decoder via the incoming ST-BUS stream. The low speed data is regenerated and output by the NRZ/RZ output circuitry. The data codec can operate in eight modes. The specific mode of operation is selected by programming the internal Control Register using the CSTi serial input.

Transmit Path

The NRZ/RZ input circuitry can be programmed to accept RZ or NRZ data by asserting the appropriate level on the DF pin (HIGH=RZ format; LOW=NRZ format).

In the RZ format, both D_X1 and D_X2 are used for the input data. MARK pulses are received on one line input and SPACE pulses on the other. The MARK and SPACE polarities of the input pins are fixed by the high to low transition of the $\overline{RxE}$ line. The input having the last transition before $\overline{RxE}$ goes low is selected to be the MARK input. Thus to ensure correct polarity selection, the data codec should be receiving MARK pulses before $\overline{RxE}$ is taken low. The $\overline{RxE}$ line must be kept low for the duration of the call. As indicated before, the Data Codec does accept violation pulses. The violation pulses can be input on the MARK or SPACE lines. The time difference between a violation pulse and an actual data pulse must be at least 125µs. Since only one violation pulse is encoded per frame, the minimum time period between consecutive pulses should be 125µs as illustrated in Figure 4.

In the NRZ format, only one line is required for the data. This is input at D_X1 (Pin 9). The second input, D_X2, can be used for transmitting secondary control information. The signal on this input pin is encoded only when there is no activity on the D_X1 line, i.e., during steady MARK or SPACE condition on the data line. To ensure proper encoder function, the signal to the D_X2 line should be applied after at least 125µs have elapsed since the last data transition on D_X1. The acceptable data format for the D_X2 input is illustrated in Figure 5. Each pulse on the line is encoded as a single transition. The minimum time period between consecutive pulses should be 125µs.

The encoding of the NRZ/RZ data to the TEM format is performed by the encoder. The 8 bit TEM words are transmitted on the outgoing ST-BUS channel via DSTo. This is a three state output which is enabled only when both $\overline{CA}$ and $\overline{F1i}$ are low (see Figure 11).

Receive Path

The 8 bit word generated by a data codec at a remote end is shifted in from the incoming ST-BUS stream via the DSTi input. The word is shifted in at the same time as the outgoing word is shifted out, i.e., when both $\overline{CA}$ and $\overline{F1i}$ are low as illustrated in Figure 11. The NRZ/RZ low speed data is regenerated by the decoder section and output via D_R1 and D_R2.

If the chip is operating in the RZ format, D_R2 transmits MARK pulses and D_R1 transmits SPACE pulses. The format of the output signal is shown in Figure 4. The width of an output pulse is nominally 35µs and cannot be altered by the user. Violation pulses will appear on the line on which they were initially inserted at the remote end.

In the NRZ format D_R1 outputs the data. The second output pin D_R2, transmits the secondary signal. Each transition in this signal represents one data pulse encoded by the remote end. An example of the type of waveform observed is illustrated in Figure 5.

The NRZ/RZ output circuitry also transmits synchronizing pulses if the data decoded from DSTi is idling (i.e., no data transitions) for more than six clock periods of the Secondary Clock (SCLK). This Secondary Clock is typically a 600Hz input to the chip. When the codec is set in the RZ format, these sync pulses will be either MARK or SPACE violation pulses, depending on the last data bit transmitted. If it is operating in the NRZ format, the sync pulses constitutes a squarewave with high and low durations of six SCLK periods. This squarewave appears at the D_R2 output pin. Synchronization pulses are transmitted until some activity is detected by the decoder or the mode of operation is changed through the Control Register.

Timing Requirements

The data codec derives all the internal timing from the 2.048 MHz clock input (C2i) and the two enable signals $\overline{F1i}$ and $\overline{CA}$. The DSTo output goes from high impedance to the value of bit 7 of the TEM

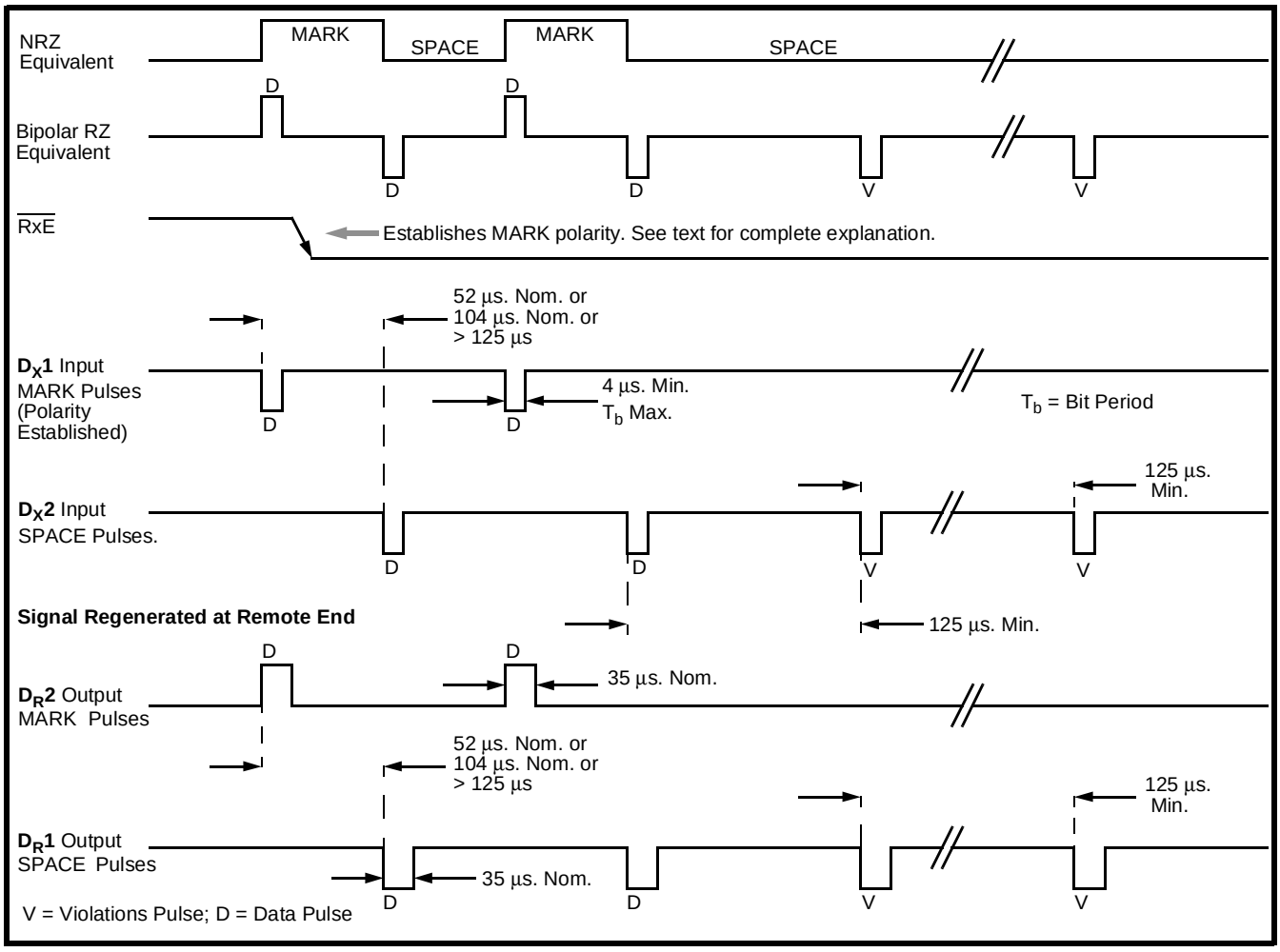


Figure 4 - Example Input/Output Waveform in the RZ format (DF=HIGH)

word on the first rising edge of the clock after $\overline{F1i}$ and $\overline{CA}$ are taken low. The 8 bit TEM word from the input ST-BUS stream is clocked into the device on the negative edge of the C2i clock. For proper codec operation, the ST-BUS interface (DSTo, DSTi, and CSTi) should be enabled for only 8 clock periods of the C2i clock in any 125µs period (one ST-BUS frame time) as shown in Figure 11. All data input and output at the ST-BUS interface takes place at 2.048 Mbps.

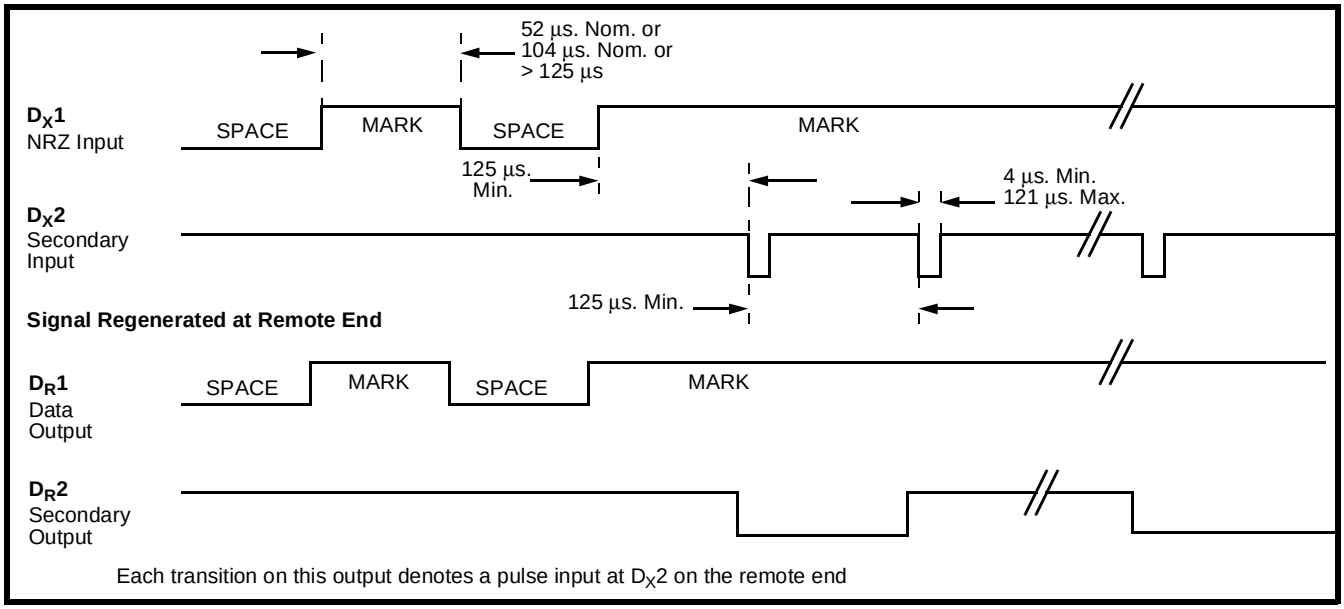


Figure 5 - Example Input/Output Waveform in the NRZ format (DF=LOW)

The Secondary Clock input (SCLK) is normally a 600Hz clock signal. This clock is internally aligned with the 2.048 MHz input. It is used to generate the synchronizing pulses and the violation word timing (when the chip is operating in the local carrier mode). Note that the 600Hz frequency is an exact multiple of the most commonly used baud rates, i.e., 300, 2400, 4800, 9600, and 19200. In synchronous data transmission schemes, the receiver timing circuitry can be kept in sync using the synchronizing pulses or the violation word when no data is being transmitted. Other clock frequencies can be used for specific applications. If this facility is not to be utilized, the SCLK input can be tied to ground.

Control Interface

An 8 bit word is read into the Control Register via the CSTi input at the same time as the TEM word is being shifted in. The chip functions controlled by the eight bits are summarized in Table 3 and described in subsequent sections.

Bit	Function
7,6,5	Device mode control bits. These bits select one of eight modes of operation
4,3,2	Violation word control bits
1	Resets the Data Activity Scan point
0	Resets the Uncommitted Scan point

Table 3. Summary of Control Register Function

Modes of Operation

As mentioned earlier, the data codec can operate in eight different modes. The specific mode is selected through bits 7, 6 and 5 in the Control Register. Table 4 summarizes the different modes.

Mode 0: Normal. This is the normal transparent conversion mode of the data codec. The NRZ/RZ input signal is directly encoded into the TEM format and output as an ST-BUS channel. The TEM word for the input ST-BUS channel is decoded and the regenerated data is output via the NRZ/RZ output circuitry. Synchronizing pulses are also transmitted as explained in the preceding paragraphs.

Mode 1: Local Carrier. In this mode the NRZ/RZ output circuitry transmits an 8 bit word at D_R2 (Pin 18) by modulating the secondary clock (SCLK). If the chip has been selected to operate in the RZ format, this word is transmitted as MARK Violations. The time interval between consecutive pulses specifies the binary value. A logical zero is represented by a time interval of one SCLK period between the pulses. A logic "1" is represented by two clock periods. In the NRZ mode, the time interval between consecutive transitions of the signal carries the information. The modulation scheme is illustrated in Figure 6. The 8 bit word consists of a sync bit followed by seven other bits. Bits 1, 4 and 5 in this word reflect the values of bits 2, 3 and 4 in the Control Register. The remaining four bits in the word are fixed as zeros. The sync bit is identified by a time interval equal to four clock periods of SCLK. The NRZ/RZ input circuitry and the encoder stage operates normally in this mode.

Control Register Bits			Mode of Operation
b7	b6	b5	
0	0	0	Normal
0	0	1	Local Carrier
0	1	0	Local Synchronization
0	1	1	Digital Loopback
1	0	0	Data Loopback
1	0	1	Data Loopback - Local Violation Word
1	1	0	Normal Mode - Drive Point Set HIGH.
1	1	1	Idle

Table 4. Modes of Operation

Mode 2: Local Synchronization. In the local sync mode, the NRZ/RZ output circuitry transmits only sync pulses on D_R2. These sync pulses appear as MARK violations in the RZ mode with the time interval between consecutive pulses equal to four SCLK periods. In the NRZ format D_R2 outputs a squarewave with a period equal to eight cycles of SCLK. D_R1 output is held at steady MARK. The NRZ/RZ input circuitry and the encoder stage of the chip function normally.

Mode 3: Digital Loopback. In this mode an 8 bit word from the incoming ST-BUS (DSTi) is sampled and one ST-BUS frame later, the same word is looped back to the corresponding outgoing channel of the ST-BUS (DSTo). This allows the user to test the ST-BUS transmission path to and from the data codec.

Mode 4: Data Loopback. This mode permits the user to test the decoding and encoding operation of the codec. A known TEM word is sent to the data codec from the ST-BUS end. This word is decoded and redirected via the output circuitry to the NRZ/RZ input circuit and subsequently to the encoder stage

for transmission out on the ST-BUS output pin (DSTo). The NRZ/RZ inputs (Pins 9 and 10) are functionally disconnected from the input circuitry. The outputs (pins 18 and 19) are in a non-active state, i.e., D_R1 is steady LOW and D_R2 is steady HIGH.

Mode 5: Data Loopback - Local Violation Word. This mode can be used for testing the operation of the chip in the local carrier mode. The Violation word is generated as in the local carrier mode. However, the modulated signal is not output on D_R2. It is rerouted to the NRZ/RZ input circuit, encoded into the TEM format and output on DSTo.

Mode 6: Normal Mode - Drive Point Activated. The drive point output (Pin 14) is set HIGH in this mode. The codec operation is normal in every other respect. This drive point can be used to control external circuitry. It is reset when the mode of operation is changed.

Mode 7: Idle. In the idle mode D_R1 and D_R2 outputs are in a non-active state, i.e., D_R1 is steady LOW and D_R2 is steady HIGH. The encoder stage and the input circuitry operates normally.

Device Monitoring Features

There are two output pins which can be used to monitor the codec.

1. **Data Activity ($\overline{DA}$):** This output goes from high to low when a SPACE signal, indicating the beginning of data activity, is received by the NRZ/RZ input circuitry. The level on this pin is reset by setting bit 1 of the Control Register to logic "1".

2. **Scan Point output ($\overline{SPo}$):** This output is set LOW whenever SPi input undergoes a low to high transition. It is reset by a logic "1" in bit 0 of the Control Register. The SPi input is generally used in conjunction with pin 11 to detect a long SPACE condition in the data. The external circuitry required to utilize this feature is illustrated in Figure 7. Note that Pin 11 ($\overline{NRZo}$) is an open drain output. The NRZ/RZ data input to the codec is converted to the NRZ format and output on this pin. The RC time constant for the circuit shown in Figure 7 can be set to detect SPACE conditions of varying time durations. The length of the long SPACE detected is given by

$$T_{SP}=0.7RC$$

Where T_{SP} is the duration of the SPACE in milliseconds. A long SPACE of 150ms is generated when the BREAK key on a data terminal is depressed. To detect this signal, a value of R equal to 210 kΩ and C equal to 1.0µF can be used.

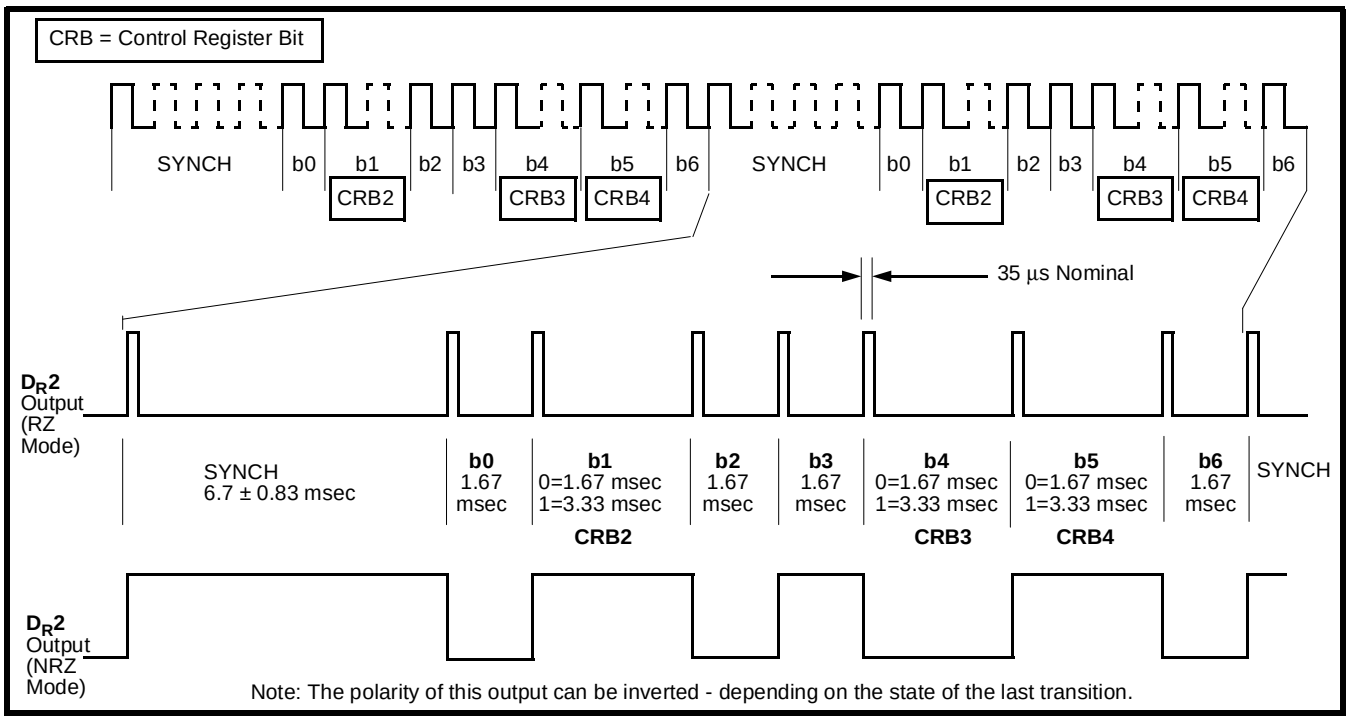


Figure 6 - Violation Word Timing in the Local Carrier Mode for a 600Hz input to SCLK

The $\overline{SPo}$ pin could then be monitored by the system processor to detect a prompt from the peripheral.

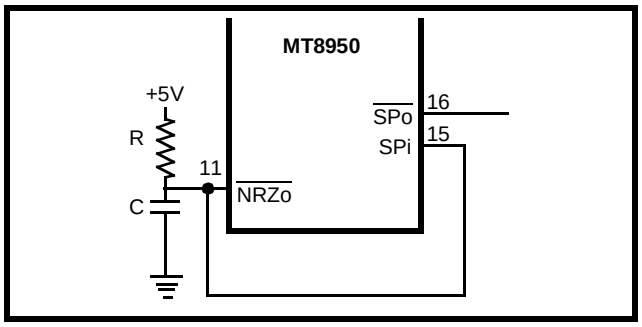


Figure 7 - Long Space Detection Circuit

External Power Reset

When the reset input ($\overline{PRST}$) is taken low, the data codec circuit goes into reset mode. The conditions present on the output pins are as follows:

1. DSTo - High Impedance
2. $\overline{SPo}$ - +5V (unasserted)
3. $\overline{DA}$ - +5V (unasserted)
4. DP - GND (unasserted)
5. D_R1 - +5V (inactive)
6. D_R2 - GND (inactive)
7. $\overline{NRZo}$ - GND (Mark condition)

The internal Control Register is loaded with HEX FF.

Applications

A block diagram schematic of a simple Voice-Data integrated switching system is illustrated in Figure 8. The data terminal can access a number of remote devices via the gateway provided by the Data Codec. In this application, the Data Codec function parallels that of the Voice Codec, i.e., the Voice

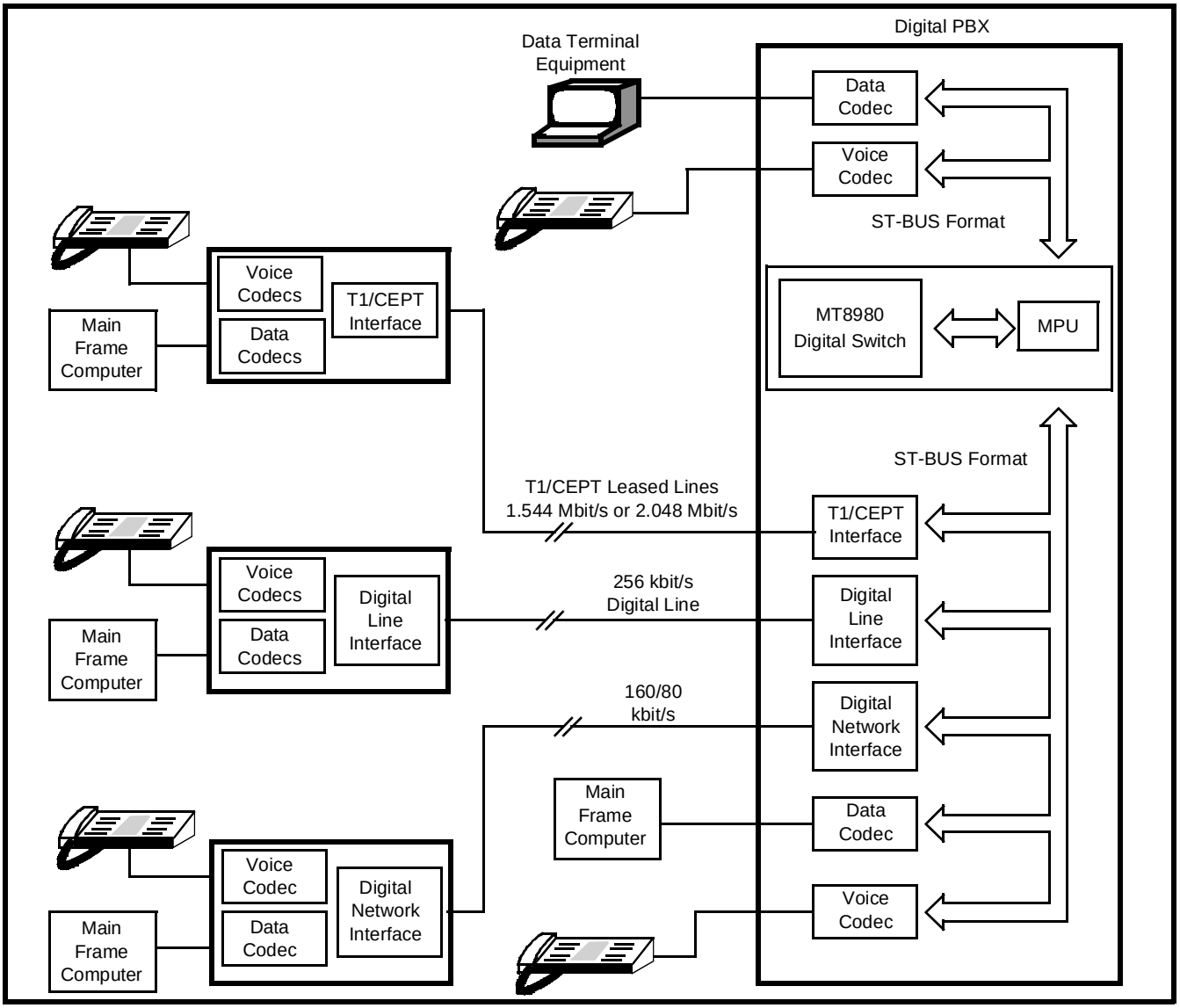


Figure 8 - Voice-Data integration using the Data Codec

Codec converts analog signals into the ST-BUS format while the Data Codec does a similar conversion for low speed data. The information in the ST-BUS format can be switched via the Digital Switch to any of the other interfaces and subsequently transmitted over the appropriate lines to the remote destination. At the remote end, the original signal is regenerated by another codec. The remote equipment can be part of a local area network or it may be accessed through leased T1/CEPT digital lines. Access to remote equipment via the T1/CEPT leased lines is acquired through the T1/CEPT interface (MT8976). Full duplex transmission at 1.544 or 2.048 Mbps is possible with this interface.

The Digital Network Interface Circuit (DNIC), the MT8972, is capable of providing 160 kbps full duplex transmission over single telephone pair wiring. This device can support two 64 kbps channels, allowing two data codecs to be interfaced to it at the remote end. Simple, low cost data sets can be constructed using the data codec and the DNIC.

A simplified interface for transmitting and receiving RS-232 data signals is illustrated in Figure 9. The Codec is selected to receive and transmit low speed data in the NRZ format. The data transmitted by the terminal equipment in the RS-232 format is inverted and level shifted to TTL-compatible levels before being fed into the D_X1 input on the Codec. The signal is converted into the ST-BUS format and transmitted via the DSTo output in one channel timeslot when the ST-BUS interface is enabled by $\overline{F1i}$ and $\overline{CA}$, as dictated by the system channel assignment scheme. During this same time period the Codec accepts the 8 bit data arriving on the incoming ST-BUS stream which is output at the STo1 pin on the MT8980. The data is decoded and the original signal input at the remote end is regenerated and output at the D_R1 pin. This signal is level shifted, inverted and transmitted to the terminal. The codec in this particular application requires no other programming. Loading of the Control Register via the CSTi input is optional. If this input is tied to ground, the Codec will operate in mode 0 (the normal mode). Note that the SCLK input is tied low. Thus synchronization pulses will not be transmitted and

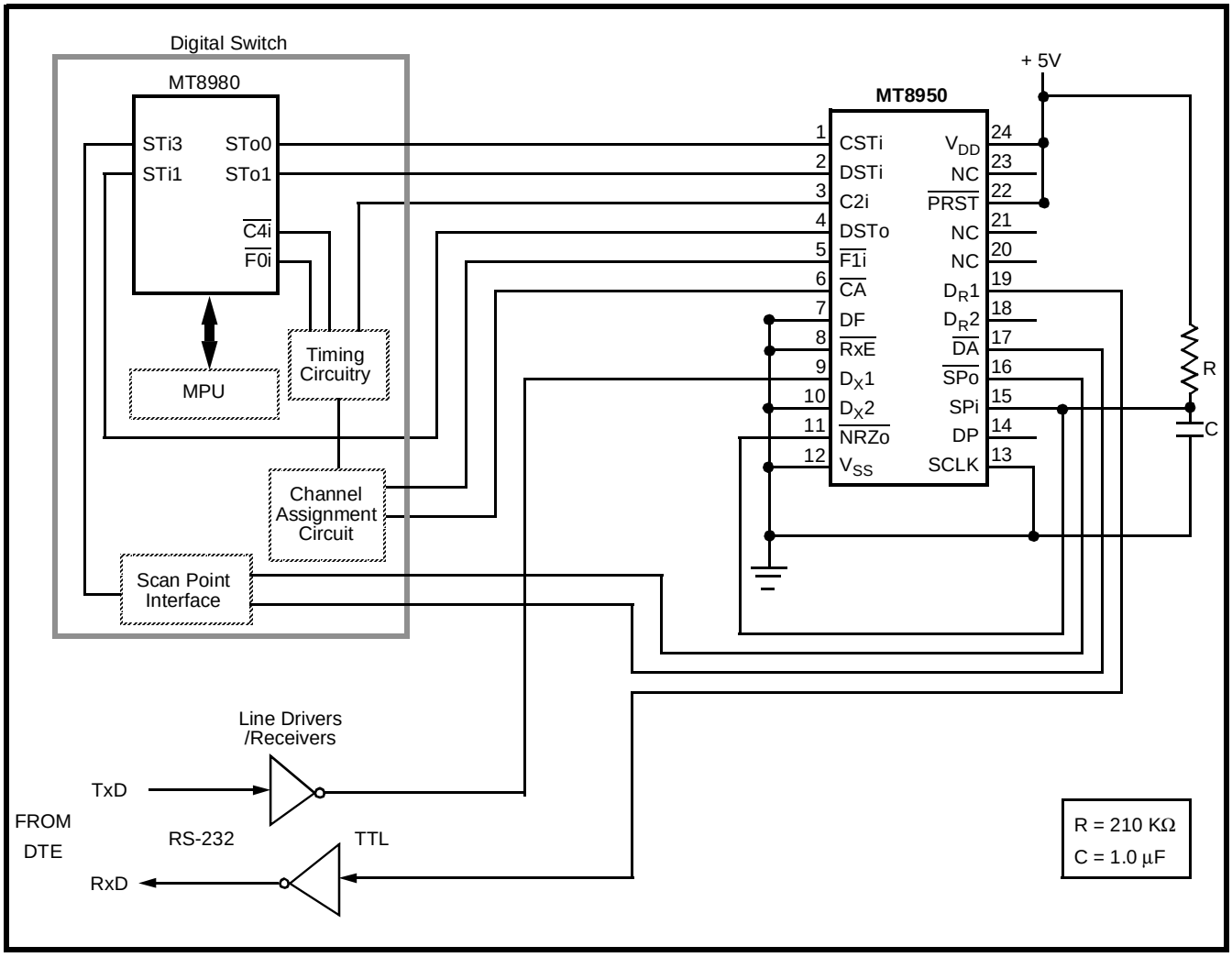


Figure 9 - Simplified RS-232 Interface using the Data Codec

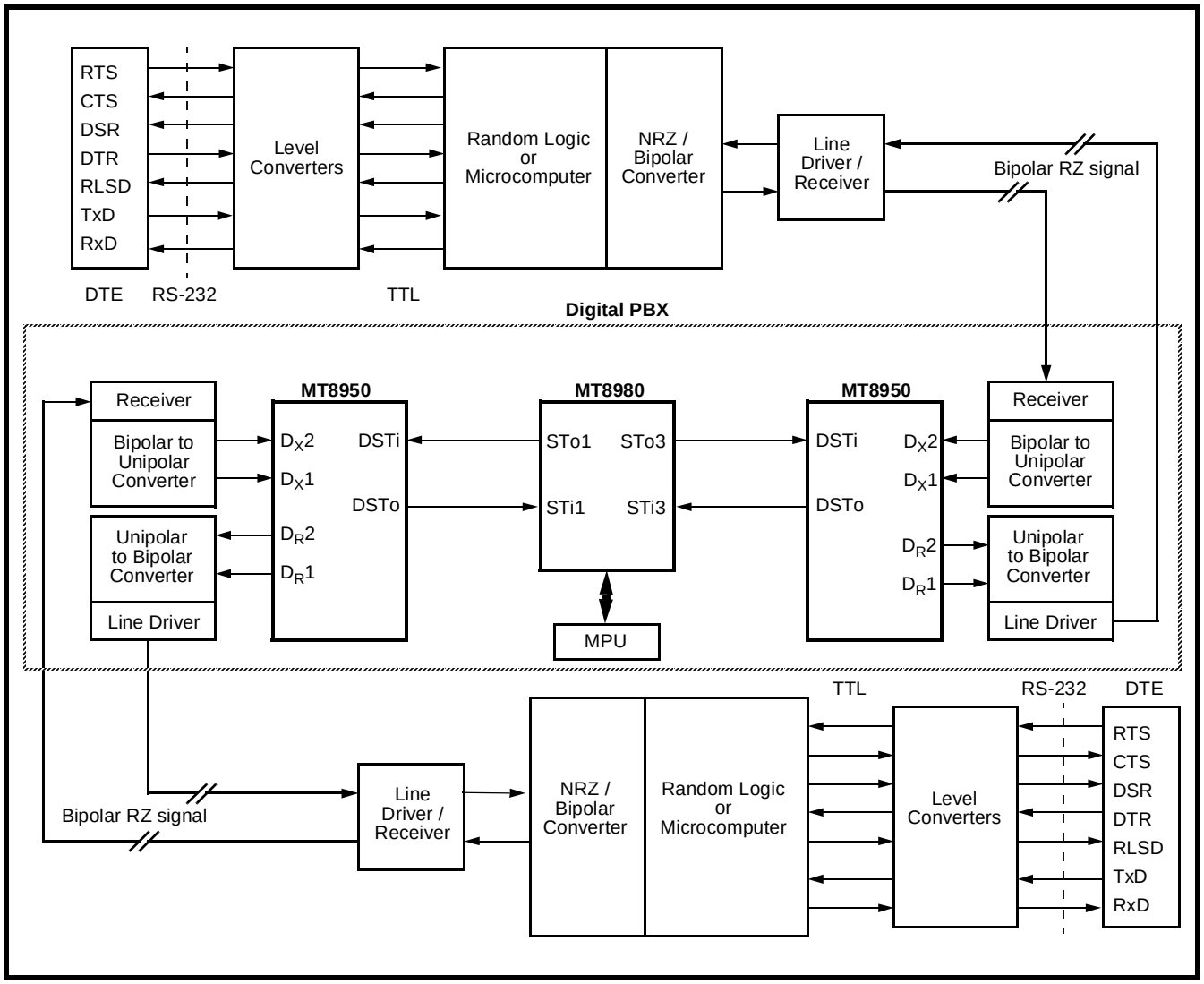


Figure 10 - Block Diagram Illustration of a Scheme to Submultiplex RS-232 Control Signals

the codec cannot be used in the local carrier mode. If this facility is to be used, an appropriate clock can be input to the device. The long SPACE detection circuitry and the Data Activity output can be used for monitoring the codec if necessary.

Figure 10 shows a block diagram schematic of a circuit which could be used to submultiplex RS-232 control signals with the data. The data and control signals are operated on by the microprocessor or the logic circuitry and subsequently transmitted as a three level signal. The control signals are encoded as bipolar violations. Since the control status does not change very frequently during a call, this information is transmitted only when no data is available. Circuitry near the Codec converts the bipolar signal into a unipolar format and inputs it at D_X1 and D_X2. Conversely, the low speed data from the Codec output at D_R1 and D_R2 is first converted to the bipolar format before being transmitted.The Data Codec is selected to operate in the RZ format.

The microprocessor or the random logic circuit examines the received signal for violations. If a stream of violations is detected, then the signal is interpreted to be control information. The detected violations are decoded and the appropriate change in the status of the RS-232 control signals is implemented. If no violations are detected then the incoming signal is considered to be the data and it is rerouted to the RxD pin of the RS-232 connector. The microprocessor could also be used in the initial call setup and for error checking of the received control information. This scheme could be used to provide transparent modem capability to any of the ST-BUS based equipment.

Absolute Maximum Ratings*

- Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	V_{DD}	-0.5	7.0	V
2	DC Input Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
3	DC Output Voltage	V_{OUT}	V_{SS}-0.3	V_{DD}+0.3	V
4	Input Diode Current (V_I<0 or V_I>V_{DD})	I_{IK}		± 10	mA
5	Output Diode Current (V_O<0 or V_O>V_{DD})	I_{OK}		± 20	mA
6	DC Output Current, per pin	I_O		± 25	mA
7	DC Supply or Ground Current	I_{DD}/I_{SS}		± 50	mA
8	StorageTemperature	T_{ST}	-65	150	^oC
9	Package Power Dissipation (CERDIP) T_A= 25^o C	P_D		1.0	W

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions

- Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Supply Voltage	V_{DD}	4.5	5.0	5.5	V	
2	Operating Frequency	f_{CK}		2.048		MHz	
3	Operating Temperature	T_A	0		70	^oC	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics

V_{DD}=5.0V±10%; V_{SS}=0V; T_A=0^{o}C to 70^{o}C - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	SUP	Quiescent Supply Current	I_{QS}			150	µA	All outputs unloaded All inputs @ V_{SS}
2	SUP	Operating supply current	I_{DD}			1.0	mA	All outputs unloaded. Input pins 2 and 3 clocked at 2.048 MHz. Pins 1,8,15,20,21 @ V_{SS} Pins 5,6,7,9,10,13 and 22 @V_{DD}
3	INPUTS	TTL inputs[1] HIGH voltage LOW voltage	 V_{IH} V_{IL}	 2.0 V_{SS}		 V_{DD} 0.8	 V V	
4	INPUTS	CMOS inputs [2] HIGH voltage LOW voltage	 V_{IH} V_{IL}	 3.5 V_{SS}		 V_{DD} 1.5	 V V	
5	INPUTS	CMOS Schmitt inputs [3] HIGH voltage LOW voltage	 V_{IH} V_{IL}	 3.0 V_{SS}		 V_{DD} 1.0	 V V	
6	INPUTS	SPi Comparator ON Voltage	V_{T+}	2.25	2.5	2.75	V	V_{DD} = 5V
7	INPUTS	SPi Comparator OFF Voltage	V_{T-}	2.0			V	V_{DD} = 5V
8	INPUTS	Input Leakage Current	I_{IN}		±1	±10	µA	V_{DD} = 5V

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

1. Include DSTi, CSTi, C2i, F1i and SCLK
2. Include $\overline{DF}$
3. Include $\overline{RxE}$,D_X1, D_X2 and $\overline{PRST}$

DC Electrical Characteristics

V_{DD}=5.0V±10%; V_{SS}=0V; T_A=0°C to 70°C - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	OUTPUTS	Output LOW voltage	V_{OL}			0.05	V	$\|I_O\|$< 1.0 µA V_{DD} = 5V
2		Output HIGH Voltage	V_{OH}	4.95			V	$\|I_O\|$< 1.0 µA V_{DD} = 5V
3		Output LOW Current (On all outputs except DSTo)	I_{OL}	2.2	2.8		mA	V_{OL}=0.4V
4		Output HIGH Current (On all outputs except DSTo)	I_{OH}	-3.5	-4.2		mA	V_{OH}=2.4V
5		Output LOW Current (On DSTo output)	I_{OL}	8.9	11.1		mA	V_{OL}=0.4V
6		Output HIGH Current (On DSTo output)	I_{OH}	-14.0	-16.8		mA	V_{OH}=2.4V
7		Output Leakage Current	I_{OZ}		±1	±10	µA	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics†

- Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		C2i Clock Frequency	f_{CK}	2.028	2.048	2.068	MHz	
2		C2i Clock Rise Time	t_{CR}			50	ns	
3		C2i Clock Fall Time	t_{CF}			50	ns	
4		Clock Duty Cycle (C2i & SCLK)			50		%	
5		SCLK Clock Frequency	f_{SCLK}	0	0.6	128	kHz	
6		SCLK Clock Rise Time	t_{SCLKR}			50	ns	
7		SCLK Clock Fall Time	t_{SCLKF}			50	ns	
8		$\overline{F1i}$ and $\overline{CA}$ Rise Time	t_{ER}			100	ns	
9		$\overline{F1i}$ and $\overline{CA}$ Fall Time	t_{EF}			100	ns	
10		$\overline{F1i}$ and $\overline{CA}$ Setup Time	t_{ES}	25			ns	
11		$\overline{F1i}$ and $\overline{CA}$ Hold Time	t_{EH}	-25		25	ns	
12		DSTo Rise Time	t_{OR}			100	ns	Note 1
13		DSTo Fall Time	t_{OF}			100	ns	Note 1
14		Propagation Delay From Clock (C2i) To Output (DSTo) enable.	t_{PZH} t_{PZL}			125	ns	Note 1
15		Propagation Delay From Clock (C2i) To Output (DSTo).	t_{PLH} t_{PHL}			125	ns	Note 1
16		Input Rise Time (DSTi, CSTi)	t_{IR}			100	ns	
17		Input Fall Time (DSTi, CSTi)	t_{IF}			100	ns	
18		DSTi, CSTi Setup Time	t_{ISH} t_{ISL}	0			ns	
19		DSTi, CSTi Hold Time	t_{IH}	90			ns	
20		$\overline{PRST}$ Low Time		488			ns	

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
Note 1: R_L=10KΩ to V_{DD}, C_L=150 pF to V_{SS}

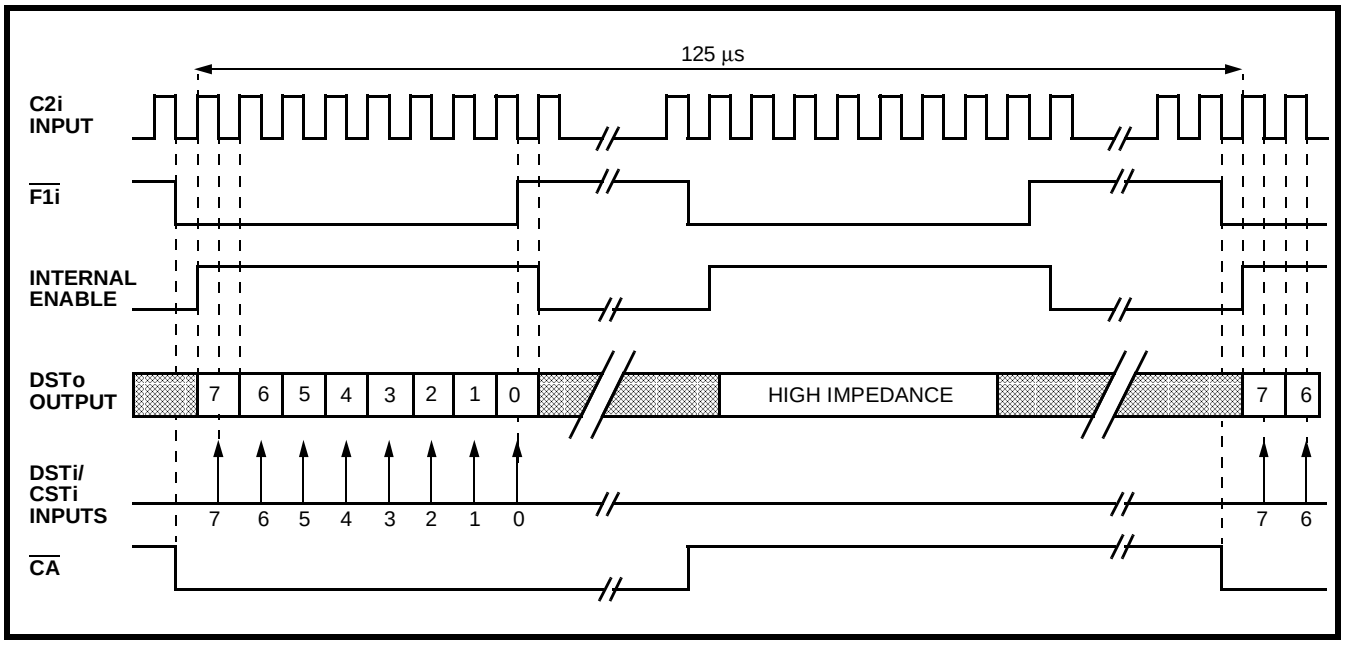


Figure 11 - Timing Diagram - 125 µs Frame Period

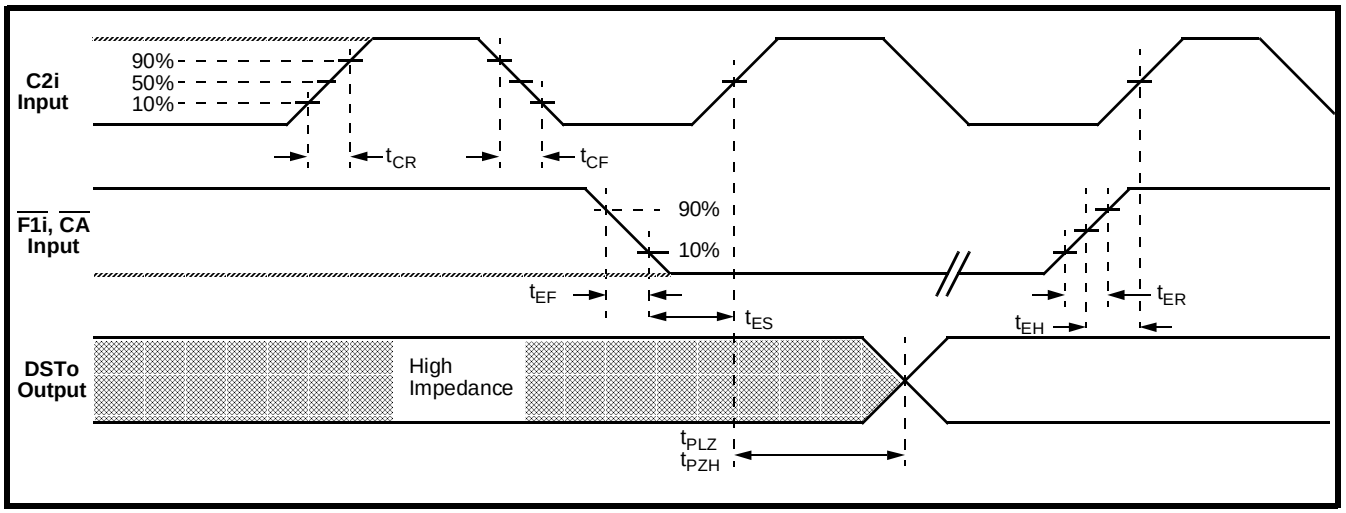


Figure 12 - Timing Diagram - ST-BUS Interface Enable

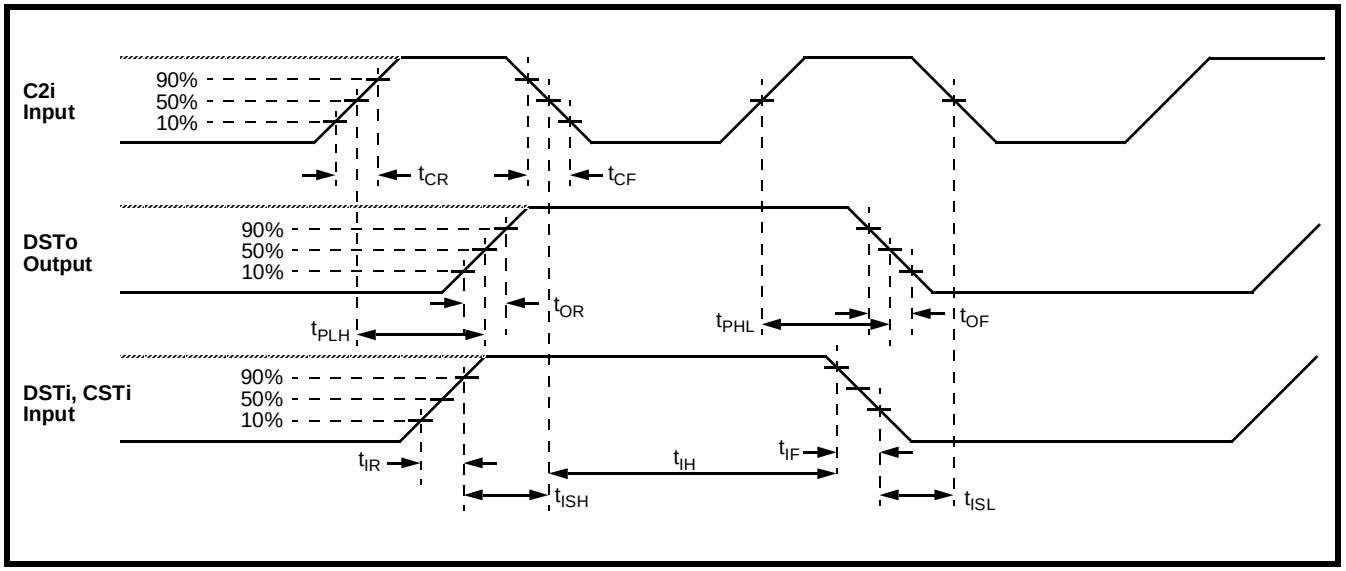


Figure 13 - Timing Diagram - ST-BUS Input/Output

NOTES: