19-1067; Rev 1, 7/96

MAXIM

Dual Universal Switched Capacitor Filter

General Description

The MF10 is a dual 2nd order, switched capacitor, state variable filter. Each of the two filter sections uses two switched capacitor integrators and an op amp to generate a second order function. The location of the poles (and thus the center frequency and Q) is determined by the frequency of an external clock and 2 to 4 external resistors. No external capacitors are used.

Each of the two filter sections of the MF10 can generate all standard 2nd order functions: bandpass, lowpass, highpass, notch (band-reject), complex zeroes and allpass functions. Three of these functions are simultaneously available. The frequency of the 2nd order poles is accurate to ±0.2% and the Q is accurate to within 2%.

Fourth order filters can be made by cascading the two 2nd order filter sections of the MF10, and higher order filters can easily be made by cascading more MF10s. The excellent accuracy and stability of MF10 based filters eliminates the complex, costly tuning normally required in the production of high order (multipole) filters. Design equations for Butterworth, Bessel, Chebyshev, and Cauer (Elliptic) filters are provided.

Features

- **No External Capacitors Required**
- **Low Sensitivity to External Component Variation**
- **Excellent Frequency and Q Stability**
- **Easily Cascaded for Multipole Filters**
- **Filter Frequency Set by External Clock Frequency**
- **0.2% Clock to Center Frequency Ratio Accuracy**
- **Highpass, Lowpass, Bandpass, Notch, and Allpass Filter Functions.**
- **Up to 3 Simultaneous Filter Function Outputs**
- **Up to 30kHz Operation**
- **Easy to use—Design Directly from the Data Sheet**
- **Monolithic, Low Power CMOS Design**

Applications

This versatile device is used for a wide range of filtering applications such as:

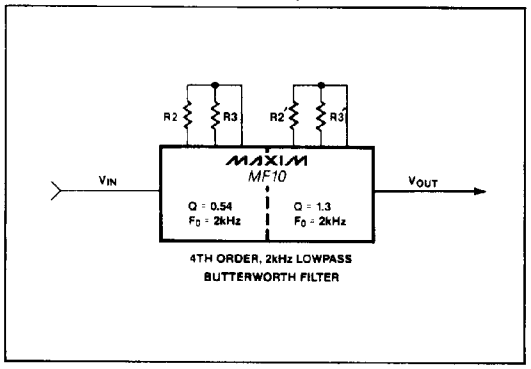
Tunable active filters
Multi-pole filters
Anti-aliasing filters
Adaptive Filtering
Phase locked loops
Signal Processing/ Conditioning

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MF10BN	0°C to +70°C	20 Lead Plastic DIP
MF10CN	0°C to +70°C	20 Lead Plastic DIP
MF10BWP	0°C to +70°C	20 Lead Wide SO
MF10CWP	0°C to +70°C	20 Lead Wide SO
MF10BJ	0°C to +70°C	20 Lead CERDIP*
MF10CJ	0°C to +70°C	20 Lead CERDIP*
MF10CC/D	0°C to +70°C	Dice*

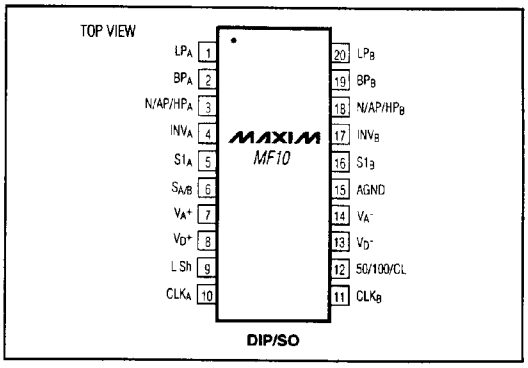
* *Contact Factory*

Typical Operating Circuit



4TH ORDER, 2kHz LOWPASS BUTTERWORTH FILTER

Pin Configuration



DIP/SO

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 14V
Power Dissipation 500mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Complete Filter)

(V_S = ±5V, T_A = +25°C)

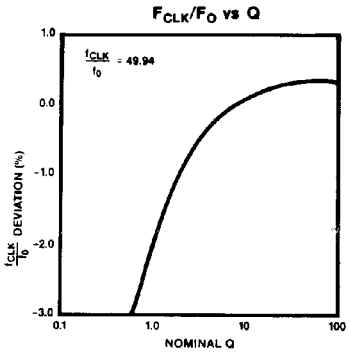
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range	$f_o \times Q \leq 200$ kHz	20	30		kHz
Clock to Center Frequency Ratio, f_{CLK}/f_o					
MF10B_	Pin 12 High, Q = 10		49.94 ± 0.2%	±0.6%	
MF10C_	$f_o \times Q \leq$ 50kHz, Mode 1		49.94 ± 0.2%	±1.5%	
MF10B_	Pin 12 at Mid Supplies		99.35 ± 0.2%	±0.6%	
MF10C_	Q = 10, $f_o \times Q \leq$ 50kHz, Mode 1		99.35 ± 0.2%	±1.5%	
Q Accuracy (Q Deviation from an Ideal Continuous Filter)	$f_o \times Q \leq$ 50kHz $f_o \leq$ 5kHz, Mode 1		±2%	±6%	
f_o Temperature Coefficient	Pin 12 High (~50:1) Pin 12 Mid Supplies (~100:1) $f_o \times Q \leq$ 100kHz, Mode 1 External Clock Temperature Independent		±10 ±100		ppm/°C ppm/°C
Q Temperature Coefficient	$f_o \times Q \leq$ 100kHz, Q Setting Resistors Temperature Independent		±500		ppm/°C
DC Low Pass Gain Accuracy	Mode 1, R1 = R2 = 10kΩ		±1	±2	%
Crosstalk			50		dB
Clock Feedthrough			10		mV
Maximum Clock Frequency		1	1.5		MHz
Power Supply Current			7	10	mA

ELECTRICAL CHARACTERISTICS (Internal Op Amps)

(V_S = ±5V, T_A = +25°C)

PARAMETER	CONDITIONS	MIN	Typ	MAX	UNITS
Supply Voltage		±4	±5		V
Voltage Swing (Pins 1, 2, 19, 20)	R_L = 5kΩ				
MF10B_		±4.0	±4.1		V
MF10C_		±3.8	±3.9		V
Voltage Swing (Pins 3 and 18)	R_L = 3.5kΩ				
MF10B_		±4.0	±4.1		V
MF10C_		±3.8	±3.9		V
Output short Circuit Current					
Source			3		mA
Sink			1.5		mA
Gain Bandwidth Product			2.5		MHz
Slew Rate			7		V/μS

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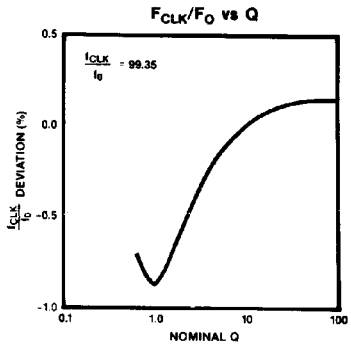


Table 1. PIN DESCRIPTION

PIN NAME	PIN NUMBER Filter A	PIN NUMBER Section B	DESCRIPTION
LP	1	20	These are the lowpass, bandpass, and notch/allpass/highpass outputs of each 2nd order section. The LP and BP outputs can typically sink 1mA and source 3mA. The N/AP/HP output can typically sink 1.5mA and source 3mA.
BP	2	19	
N/AP/HP	3	18	
INV	4	17	INV is the inverting input of the summing op amp of each filter.
S1	5	16	This is an alternate signal input pin used in modes 1A, 4, 5 and 6B. This pin must be driven with a low source impedance.
$S_{A/B}$	6		The $S_{A/B}$ input controls a switch connecting one of the inputs of the filter's 2nd summer — either to analog ground ($S_{A/B}$ low) or to the low pass output ($S_{A/B}$ high). The $S_{A/B}$ input controls the configuration of both sections of the MF10.
V_A^+	7		Analog and digital positive supply inputs.
V_D^+	8		These pins are internally connected through the MF10's substrate and therefore V_A^+ and V_D^+ should be derived from the same power supply source.
L_S			Level shift pin. This pin controls the digital input threshold level of the clock inputs, CLK_A and CLK_B. With the level shift pin at 0V and with ±5V power supplies, the clock inputs are TTL compatible. With the level shift pin connected to V_D^- the clock input thresholds are approximately 2V above V_D^-.

PIN NAME	PIN NUMBER Filter A	PIN NUMBER Section B	DESCRIPTION
CLK	10	11	Clock inputs for each switched capacitor building block. The duty cycle should be close to 50% to allow the op amps the maximum time to settle, particularly when the clock frequency is above 200kHz.
50/100/CL	12		This three-level input pin selects one of three MF10 operating conditions. When the 50/100/CL pin is connected to V_D^+ the ratio between clock frequency and center frequency is 50:1. With this pin at mid supplies (i.e., analog ground with dual supplies) the clock frequency to center frequency ratio is 100:1. Tying the pin low activates a simple current limiting circuitry which halts normal filtering operation and reduces the supply current by 70%.
V^-	13		Analog and digital negative supply inputs. These pins are internally connected. V_A^- and V_D^- should be derived from the same power supply source.
V_A^-	14		
AGND	15		Analog Ground. This pin should be connected to the system ground for dual supply operation or driven to mid supply for single supply operation. The non-inverting inputs of the filter op amps are internally connected to the AGND pin, therefore AGND should be well bypassed

Dual Universal Switched Capacitor Filter

Definition of Terms

f_{CLK}: The frequency applied to the switched capacitor filter external clock input.

f_0: The center frequency of the second order complex pole pair, f_0, is determined by measuring the peak response frequency at the bandpass output.

Q: "Quality factor", or Q, is the ratio of f_0 to the -3dB bandwidth of the second order bandpass filter. Q also determines the amount of amplitude peaking at the lowpass and highpass outputs, but is not measured at these outputs.

H_{OBP}: The gain in V/V of the bandpass output at $f=f_0$. See Figure 1.

H_{OLP}: The gain in V/V of the lowpass output as f—0Hz, See Figure 2.

H_{OHP}: The gain in V/V of the highpass output at $f = f_{CLK}/2$. See Figure 3.

Q_Z: The quality factor of the 2nd order function complex zero pair, if any.

f_z: The center frequency of the 2nd order complex zero pair. If f_z is different from f_0, and Q_z is high, f_z can be observed as a notch frequency at the allpass output.

f_{notch}: The frequency of minimum amplitude response at the notch output.

H_{OCZ1}: The complex zero output gain as f—0Hz.

H_{OCZ2}: The complex zero output gain at $f = f_{CLK}/2$.

H_{ON1}: The notch output gain as f —0Hz.

H_{ON2}: The notch output gain at $f = f_{CLK}/2$.

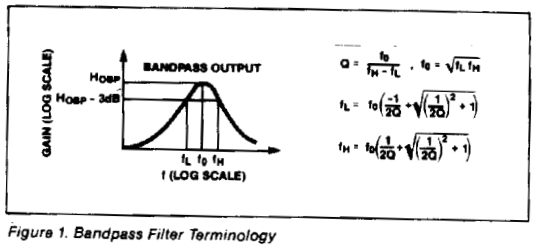


Figure 1. Bandpass Filter Terminology

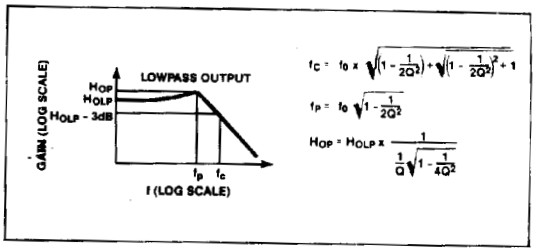


Figure 2. Lowpass Filter Terminology

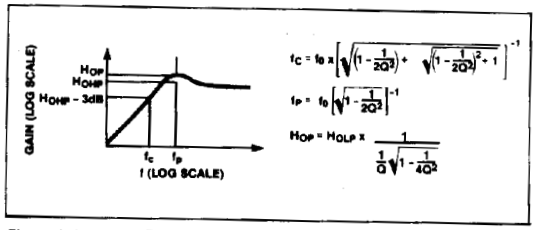


Figure 3. Highpass Filter Terminology

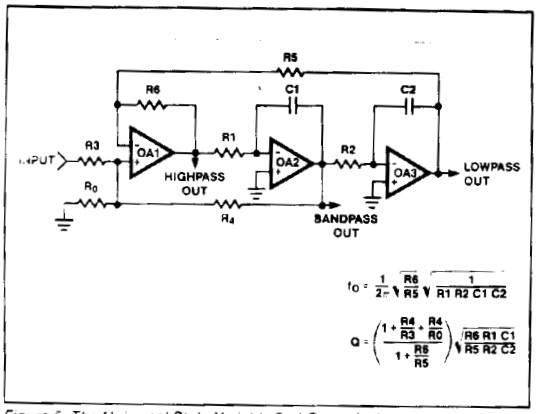


Figure 5. The Universal State Variable 2nd Order Active Filter Using RC Integrators

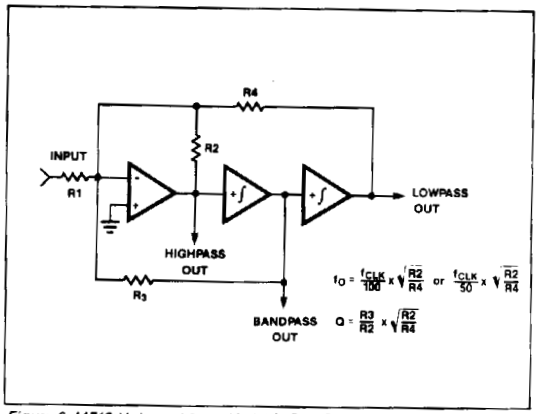


Figure 6. MF10 Universal State Variable 2nd Order Active Filter (Mode 3)

Dual Universal Switched Capacitor Filter

General Description

The MF10 is a switched capacitor (sampled data) filter. While the time domain approach most accurately describes the MF10's transfer functions, time domain calculations are cumbersome and most circuit designers are more familiar with the frequency domain approach used in designing RC active filters. Fortunately, the MF10 closely emulates RC active filters when the sampling frequency is much higher than the frequency band of interest. The operation of the MF10 can then be described in terms of the frequency domain with reasonable accuracy. Specifically, each of the two sections of an MF10 can be treated as a second order state variable filter. The similarity between the MF10 and the classic state variable filter allows the use of the extensive literature available on the design of 2nd order state variable filters.

The RC second order state variable filter (Figure 5) requires 3 op amps, 7 resistors, and 2 capacitors. This filter lacks the frequency stability and tunability of the MF10 switched capacitor filter. The MF10 excels in these areas because the center frequency of a switched capacitor filter is determined by the frequency of the clock, which, if crystal controlled, can achieve a stability of a few parts per million over the entire operating temperature range. Having the center frequency controlled by an external digital clock frequency also simplifies tuning of the filter since it is easier to accurately control a variable modulo divider than it is to precisely vary the time constant of an RC integrator.

The MF10's maximum guaranteed operating clock frequency is 1MHz, corresponding to a 20kHz maximum filter center frequency with a 50:1 clock to center frequency ratio, and a 10kHz maximum center frequency with a 100:1 clock to center frequency ratio.

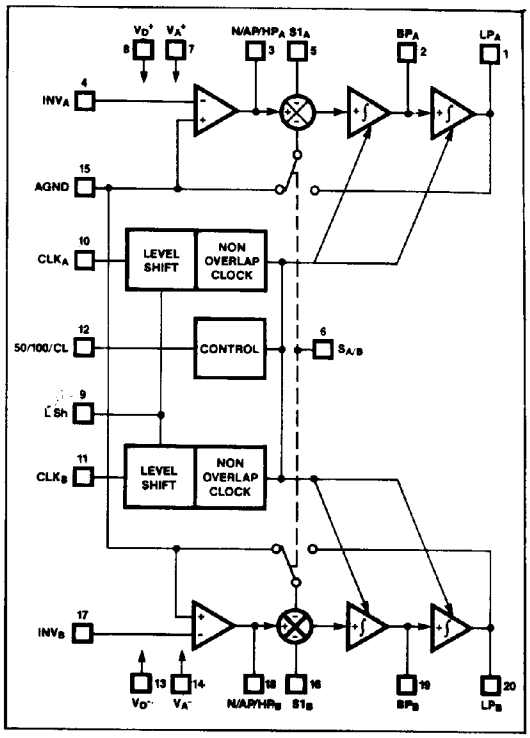


Figure 4. Block Diagram of the MF10

Filter Design

Simple 2nd Order Bandpass Filter Design

All modes except mode 6 offer a 2nd order bandpass response. The simplest circuit, mode 1A uses only two external resistors, but is limited to low Q operation by output swing limitations. Mode 1 uses three resistors and is suitable for either low or high Q bandpass functions. The center frequency of modes 1 and 1A is determined solely by the external clock frequency. Modes 2 and 3 are also suitable for bandpass filters, and are easier to implement in some applications since the center frequency is controlled by both the external clock frequency and a resistor ratio. See Table 2.

Second order bandpass filter functions are characterized by Q, center frequency, and gain (or amplitude response). Resistor selection should follow these steps, using the design equations for the selected mode:

1) Pick a value for R2, typically 10 to 100 kΩ.

2) For modes 2 and 3 only, determine the value of R4 using the available external clock frequency and the selected value for R2. (The center frequency of mode 1 and 1A is determined solely by the external clock frequency.)

3) Determine the value of R3, using the desired Q and the previously determined values of R2 and R4.

4) Determine the value of R1 required to obtain the desired filter gain.

Table 2. MODE SELECTION

FILTER TYPE	MODE
Lowpass	1, 1A, 2, 3, 3A, 4, 5, 6A, 6B
Highpass	3, 3A, 6A
Bandpass	1, 1A, 2, 3, 3A, 4, 5
Notch	2, 3A, 5 (Complex Zero)
Allpass	4, 5

Dual Universal Switched Capacitor Filter

Table 3A. NORMALIZED LOWPASS FILTER PARAMETERS

NUMBER OF POLES	BUTTERWORTH		BESSELL		CHEBYSHEV					
					0.1dB RIPPLE		0.5dB RIPPLE		2dB RIPPLE	
	fn	Q	fn	Q	fn	Q	fn	Q	fn	Q
2	1.0	0.707	1.274	0.577	1.820	0.767	1.231	0.864	0.907	1.129
3	1.0	Real Pole	1.325	Real Pole	0.969	Real Pole	0.625	Real Pole	0.369	Real Pole
	1.0	1.000	1.450	0.691	1.300	1.341	1.069	1.706	0.941	2.552
4	1.0	0.541	1.432	0.522	0.789	0.619	0.597	0.705	0.471	0.929
	1.0	1.307	1.606	0.806	1.153	2.183	1.031	2.941	0.964	4.594
5	1.0	Real Pole	1.505	Real Pole	0.539	Real Pole	0.362	Real Pole	0.218	Real Pole
	1.0	0.618	1.559	0.564	0.797	0.915	0.690	1.178	0.627	1.775
	1.0	1.618	1.758	0.917	1.093	3.282	1.018	4.545	0.976	7.232
6	1.0	0.518	1.607	0.510	0.513	0.599	0.396	0.684	0.316	0.902
	1.0	0.707	1.692	0.611	0.834	1.332	0.768	1.810	0.730	2.844
	1.0	1.933	1.908	1.023	1.063	4.633	1.011	6.513	0.983	10.462
7	1.0	Real Pole	1.687	Real Pole	0.377	Real Pole	0.256	Real Pole	0.155	Real Pole
	1.0	0.555	1.719	0.532	0.575	0.846	0.504	1.092	0.461	1.646
	1.0	0.802	1.82	0.661	0.868	1.847	0.823	2.575	0.797	4.115
	1.0	2.247	2.053	1.126	1.045	6.233	1.008	8.842	0.987	14.280
8	1.0	0.510	1.781	0.506	0.382	0.593	0.297	0.677	0.238	0.892
	1.0	0.601	1.835	0.560	0.645	1.183	0.599	1.611	0.572	2.533
	1.0	0.900	1.956	0.711	0.894	2.453	0.861	3.466	0.842	5.584
	1.0	2.563	2.192	1.226	1.034	8.082	1.006	11.530	0.990	18.687

The normalized frequencies for the Butterworth and Bessel filters are for a -3dB frequency of 1Hz. The Chebyshev and Elliptic normalized frequencies are for filters whose amplitude response passes from the ripple band to the stopband at 1Hz.

Simple Lowpass Filter Design

Use mode 6 or 6A if a single pole lowpass filter is desired (such as the odd pole in an odd-ordered complex filter). Single pole resistor values are determined using the equations for modes 6 and 6A:

1) Select a value for R2, typically 10 to 100 kΩ.

2) Determine R3, using the selected value of R2, the available external clock frequency, and the desired cutoff frequency.

3) Determine the value of R1 to obtain the desired gain.

Modes 1 and 1A, with a fixed clock to cutoff frequency, are the simplest 2nd order lowpass configurations. Modes 2 and 3 allow tuning of the cutoff frequency by either changing the clock frequency or adjusting resistor ratios.

Second order lowpass filter functions are characterized by Q, cutoff frequency, and gain (or amplitude response). Resistor selection should follow these steps, using the design equations for the selected mode:

1) Pick a value for R2, typically 10 to 100 kΩ.

2) For modes 2 and 3 only, determine the value of R4 using the available external clock frequency and the selected value for R2. (The cutoff frequency of mode 1 and 1A is determined solely by the external clock frequency.)

3) Determine the value of R3, using the desired Q and the previously determined values of R2 and R4.

4) Determine the value of R1 required to obtain the desired filter gain.

Simple Highpass Filter Design

Use mode 3 or 3A to implement 2nd order highpass filters and mode 6 for a single pole highpass filter.

Second order highpass filter functions are characterized by Q, cutoff frequency, and gain (or amplitude response). Resistor selection should follow these steps, using the design equations for the selected mode:

1) Pick a value for R2, typically 10 to 100 kΩ.

2) For modes 3 and 3A, determine the value of R4 using the available external clock frequency and the selected value for R2.

3) Determine the value of R3, using the desired Q and the previously determined values of R2 and R4.

4) Determine the value of R1 required to obtain the desired filter gain.

Multi-pole Filter Design

The two 2nd order filter sections of the MF10 can be cascaded to obtain a 4th order (4 pole) filter response. Several MF10s can be cascaded to get very high order filter responses. Unlike filters based on RC time constants, MF10-based filters usually do not require tuning of each section since the Q and center frequencies are precisely controlled by the external clock frequency and the ratio of external resistors.

The information included here is for the most common types of multi-pole filters: Butterworth, Bessel, Chebyshev, and Elliptic or Cauer. The design information given is for a 1Hz lowpass filter. However this filter can be transformed to any desired filter type and frequency using the following steps:

Table 3B. CAUER OR ELLIPTICAL FILTER PARAMETERS

NUMBER OF POLES	STOPBAND EDGE FREQUENCY / PASSBAND EDGE FREQUENCY = 1.5, PASSBAND RIPPLE = 0.5dB				STOPBAND EDGE FREQUENCY / PASSBAND EDGE FREQUENCY = 2.0, PASSBAND RIPPLE = 0.5db				STOPBAND EDGE FREQUENCY / PASSBAND EDGE FREQUENCY = 3.0, PASSBAND RIPPLE = 0.5dB			
	F_n	Q	F_z	A_{min} (dB)	F_n	Q	F_z	A_{min} (dB)	F_n	Q	F_z	A_{min} (dB)
2	1.266	0.969	1.982	8.3	1.262	0.803	2.732	13.9	1.247	0.737	4.182	21.5
3	0.707 1.072	Real Pole 2.208	1.675	21.9	0.693 1.072	Real Pole 1.859	2.27	31.2	0.653 1.070	Real Pole 1.697	3.439	42.8
4	1.03 0.687	3.922 1.087	1.592 3.478	36.2	1.031 0.641	3.32 1.13	2.143 4.992	48.6	1.031 0.615	3.032 1.159	3.3233 7.647	64.2
5	0.426 1.016 0.759	Real Pole 6.118 1.754	1.557 2.332	50.6	0.393 1.017 0.725	Real Pole 5.193 1.723	2.089 3.251	66.1	0.375 1.017 0.705	Real Pole 4.747 1.711	3.146 5.008	85.5

1) Identify the type of transfer function (lowpass, highpass, bandpass, etc.); the type of response (Butterworth, Bessel, Chebyshev, etc.); the number of poles, and the cutoff frequency.

2) Determine the normalized lowpass filter frequency and Q of each filter section, using Table 3A or 3B.

3) If a multi-pole transfer function other than lowpass is desired, perform the filter type transformation, as described below.

4) Denormalize each filter section frequency, fn, by multiplying the fn by the actual desired cutoff or center frequency.

5) Select a mode of operation for each filter section. Mode 3 is suitable for most filters, including Bessel and Chebyshev. Butterworth filters can be implemented using either mode 3 or mode 1. Elliptical filters can be implemented using modes 2 and 3A. Modes 6 and 6A provide a single, real pole needed for odd-ordered transfer functions. Allpass and complex zeroes can be generated in modes 4 and 5.

6)Select a clock frequency. The ratio of clock frequency to center frequency can be adjusted with resistor ratios in modes 2,3,5 and 6; allowing the use of any conveniently available clock frequency that is approximately 20 to 200 times the desired cutoff or center frequency.

7) Determine the resistor values for each filter section, using the design procedures given in the sections above for simple 2nd order bandpass, lowpass and highpass filters.

Tables 3A and 3B gives the normalized filter frequency and Q for each second order section of a multi-pole filter. Filters with an odd number of poles have one entry with "real pole" in the Q column. This denotes a real pole that should be implemented using mode 6 or a simple RC section.

Lowpass to Highpass Transformation.

The cutoff frequency and Q of each lowpass section is transformed using these equations:

$$f_n(\text{highpass}) = \frac{1}{f_n(\text{lowpass})}$$

$$Q(\text{highpass}) = Q(\text{lowpass})$$

Lowpass to Bandpass Transformation.

If the ratio between the upper and lower -3dB cutoff frequencies is greater than 1.5, the best way to make the desired bandpass filter is to cascade a lowpass filter and a highpass filter. The lowpass filter's cutoff frequency should be set to the desired bandpass upper cutoff frequency, and the highpass filter's cutoff frequency should be set to the desired bandpass filter lower cutoff frequency.

For very narrowband filters, several sections with identical center frequencies can be cascaded. When identical bandpass filters are cascaded, the Q of the resultant filter is

$$Q = \frac{Q}{\sqrt{2^n - 1}}$$

where Q is the Q of each individual filter section, B is the bandwidth of each individual filter section, and n is the number of identical sections cascaded. See table 4.

Table 4. CASCADING IDENTICAL BANDPASS FILTER SECTIONS

NUMBER OF IDENTICAL BANDPASS SECTIONS	BANDWIDTH	Q
1	1.000 B	1.00 Q
2	0.644 B	1.55 Q
3	0.510 B	1.96 Q
4	0.435 B	2.30 Q
5	0.386 B	2.60 Q

Dual Universal Switched Capacitor Filter

Application Hints

1) The maximum output swing is typically to within 1V of either supply rail. Check the peak amplitude response gains, H_{OBP}, H_{OLP}, H_{OHP}, and the input signal level to ensure that the outputs will not be driven beyond their maximum output swing range. This caution particularly applies to mode 1A when used with high Q values. The section labeled "Circuit Dynamics" is included in the description of each mode to clarify the relationship between the various filter parameters and the output amplitude peaking at the filter outputs. The lower Q sections of cascaded filters should precede the sections with high Q. This reduces the possibility of output clipping.

2) The absolute values of resistors are not critical, only the ratios between resistors directly affect filter operation. The absolute values must be high enough so that the output drive currents do not approach the limits of 3mA source current and 1mA sink current. At the other extreme, resistor values should not be so high that stray leakage currents and stray capacitances have a significant effect on circuit operation.

3) Selecting 100:1 operation doubles the number of samples per output cycle, and halves the number of output steps compared to 50:1 operation. On the other hand, 50:1 allows higher frequency operation (20kHz max vs. 10kHz max), and also offers better center frequency stability (±10ppm/°C vs. ±100ppm/°C).

4) The minimum frequency of operation is limited by the rate of discharge of the internal switched capacitors. The droop rate at the output of the integrators will be approximately 0.1mV/ms. This limits the lower value of clock frequency to about 100Hz for reasonable accuracy, corresponding to a center frequency of 1Hz using the 100:1 mode.

5) For the best accuracy in setting the center frequency, use the corrections shown in the Typical Operating Characteristic graphs. These graphs aid in the correction for the slight interaction between clock frequency, Q, and center frequency.

6) As with all sampled data systems, high frequency components of the input signal above half the clock rate will be aliased. In particular, input signal components with frequencies near the clock rate will generate difference frequencies that may fall within the passband of the lowpass and bandpass filters. Since the ratio of clock frequency to center frequency is approximately 50:1 or 100:1, a simple one pole passive RC filter will be sufficient filtering in many cases. In many other cases the input signal will itself be band-limited and will not require additional filtering.

7) The $S_{A/B}$ input controls the source of feedback into the three input summer of both sections of the MF10. If your design requires that the input of one section's summer be grounded and the input to the other section's summer be connected to the lowpass output, check to see if $S_{A/B}$ can be connected to V_D^- and the lowpass output connection made via the $S1_A$ (or $S1_B$) input.

8) If large input voltage signals are applied to the filter, the DC offset voltages of the MF10 may cause output clipping. For a more detailed discussion see the section on DC Offsets.

9) For best results, the positive and negative supplies should be bypased to AGND with a 10μF tantalum and 0.1μF ceramic capacitors.

Mode 1A
Non-Inverting Bandpass, Inverting Bandpass, Lowpass.

This minimum component count configuration uses only two external resistors. The peak gain at the inverting bandpass output is equal to the Q times the input voltage, so this circuit should only be used for low Q applications. The ratio of bandpass center frequency to clock frequency is fixed at either 50:1 or 100:1, as selected by the 50/100/CL input.

Design Equations

$$f_0 = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

$$Q = \frac{R3}{R2}$$

$$H_{OLP} = -1$$

$$H_{OBP1} = -\frac{R3}{R2}$$

$$H_{OBP2} = 1 \text{ (non-inverting)}$$

Circuit Dynamics

$H_{OBP1} = Q$ (this is the reason for the low Q recommendation)

$H_{OLP\ (peak)} = Q \times H_{OLP}$ (for high Qs)

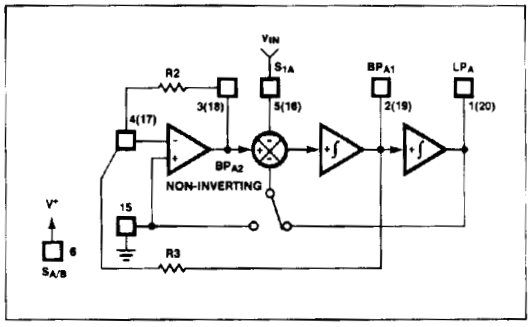


Figure 7. Mode 1A

Dual Universal Switched Capacitor Filter

Mode 1
Notch, Bandpass, and Lowpass

Like Mode 1A, f_0 is fixed at $f_{CLK}/50$ or $f_{CLK}/100$. The gain at all three outputs is inversely proportional to the value of R1; and unlike Mode 1A, high Q bandpass filters can be built without exceeding the output swing range of the bandpass output amplifier. The notch and bandpass center frequencies are identical. The notch output gain is the same above and below the notch center frequency.

Design Equations

$$f_0 = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

$$f_{notch} = f_0$$

$$Q = \frac{R3}{R2}$$

$$H_{OLP} = -\frac{R2}{R1}$$

$$H_{OBP} = -\frac{R3}{R1}$$

$$H_{ON}\left(\text{as } f \to 0\right) = -\frac{R2}{R1}$$

$$H_{ON}\left(\text{at } f = \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1}$$

Circuit Dynamics

$H_{OBP} = H_{OLP} \times Q = H_{ON} \times Q$

$H_{OLP(peak)} = Q \times H_{OLP}$ (if the DC gain of the LP output is too high, a high Q value could cause clipping at the lowpass output resulting in gain non-linearity and distortion at the bandpass output).

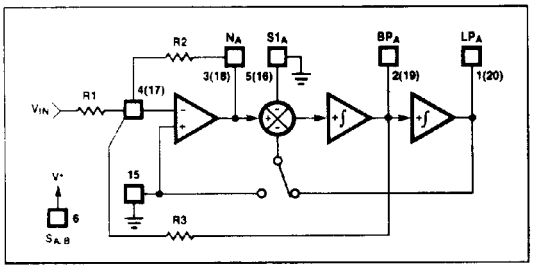


Figure 8. Mode 1

Mode 2
Notch, Bandpass, and Lowpass

The circuit of mode 2 is created by adding resistor R4 to the circuit of mode 1. This fourth resistor causes the ratio of the bandpass center frequency to clock frequency to be less than the fixed 50:1 or 100:1 ratio of mode 1. Stated another way, R4 allows the center frequency of the bandpass filter to be tuned to a higher frequency while maintaining a constant clock frequency. The notch frequency remains at $f_{CLK}/50$ or $f_{CLK}/100$, making mode 2 suitable for elliptic highpass filters, where the complex zero pair (f_{notch}) must be lower than the complex pole (f_0).

Design Equations

$$f_0 = \frac{f_{CLK}}{100} \times \sqrt{1 + \frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{1 + \frac{R2}{R4}}$$

$$f_n = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50} \quad ; \quad Q = \frac{R3}{R2} \times \sqrt{1 + \frac{R2}{R4}}$$

$$H_{OLP} = \frac{-\frac{R2}{R1}}{1 + \frac{R2}{R4}} \quad ; \quad H_{OBP} = -\frac{R3}{R1}$$

$$H_{ON1}\ (\text{as } f - 0) = \frac{-\frac{R2}{R1}}{1 + \frac{R2}{R4}}$$

$$H_{ON2}\left(\text{at } f = \frac{f_{CLK}}{2}\right) = \frac{R_G}{R_H} \times H_{OHP}$$

Circuit Dynamics

$$H_{OBP} = Q\sqrt{H_{OLP} \times H_{ON_2}} = Q\sqrt{H_{ON_1} \times H_{ON_2}}$$

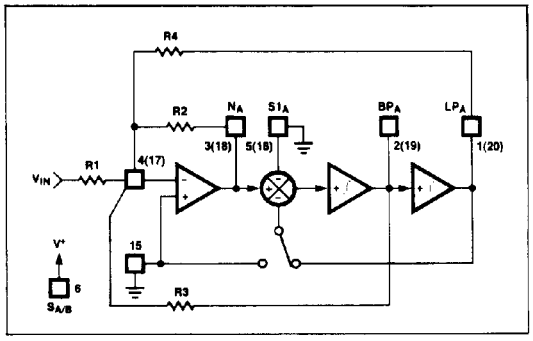


Figure 9. Mode 2

Dual Universal Switched Capacitor Filter

Mode 3
Highpass, Bandpass, and Lowpass

This mode is a sampled time (Z transform) equivalent of the classical 2nd order state variable filter. In this versatile mode, the ratio of resistors R2 and R4 can move the center frequency both above and below the $f_{CLK}/50$ and $f_{CLK}/100$ values. Mode 3 is commonly used to make multiple pole Chebyshev filters with a single clock frequency. A small (10-100pF) capacitor in parallel with R4 may be needed to avoid Q enhancement.

Design Equations

$$f_0 = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$$

$$Q = \frac{R3}{R2} \times \sqrt{\frac{R2}{R4}}$$

$$H_{OHP} = -\frac{R2}{R1}$$

$$H_{OBP} = -\frac{R3}{R1}$$

$$H_{OLP} = -\frac{R4}{R1}$$

Circuit Dynamics

$$H_{OHP} = H_{OLP}\left(\frac{R2}{R4}\right)$$

$$H_{OLP(peak)} = Q \times H_{OLP}$$

$$H_{OBP} = Q\sqrt{H_{OHP} \times H_{OLP}}$$

$$H_{OHP(peak)} = Q \times H_{OHP}$$

Mode 3A
Highpass, Bandpass, Lowpass, and Notch

Similar to mode 3, this mode adds an external op amp. This op amp creates a notch output by summing the highpass and lowpass outputs of the MF10. The ratio of resistors R_H and R_L adjusts the notch frequency, while R2 and R4 adjust the bandpass center frequency. Since the notch (zero pair) frequency can be adjusted to both above and below f_0, mode 3A is suitable for both lowpass and highpass elliptic or Cauer filters. In multipole elliptic filters only one external op amp is needed. Use the inverting input of the internal op amp as the summing node for all but the final section of the filter.

Design Equations

$$f_0 = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$$

$$Q = \frac{R3}{R2} \times \sqrt{\frac{R2}{R4}}$$

$$f_{notch} = \frac{f_{CLK}}{100} \times \sqrt{\frac{R_H}{R_L}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{\frac{R_H}{R_L}}$$

$$H_{OHP} = -\frac{R2}{R1} \quad H_{OLP} = -\frac{R4}{R1} \quad H_{OBP} = -\frac{R3}{R1}$$

$$H_{ON}\ (\text{at } f = f_0) = \left|Q\left(\frac{R_G}{R_L} H_{OLP} - \frac{R_G}{R_H} H_{OLP}\right)\right|$$

$$H_{ON1}\ (\text{as } f \to 0) = \frac{R_G}{R_L} \times H_{OLP}$$

$$H_{ON2}\left(\text{at } f = \frac{f_{CLK}}{2}\right) = \frac{R_G}{R_H} \times H_{OHP}$$

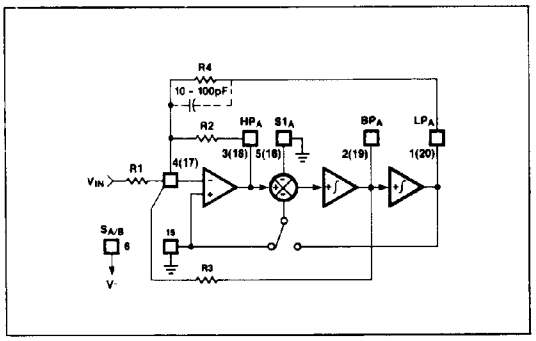


Figure 10. Mode 3

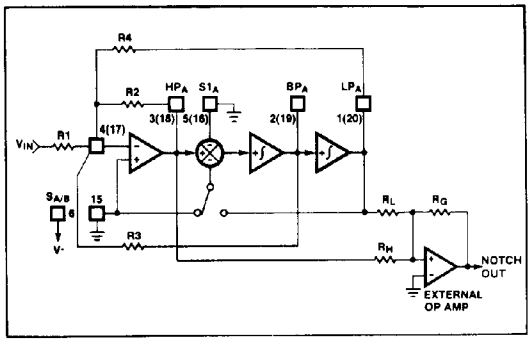


Figure 11. Mode 3A

Mode 4
Allpass, Bandpass, and Lowpass

Mode 4 provides an allpass output which has a nearly flat amplitude response with a phase shift that changes linearly with frequency (a constant time delay). For a flat amplitude response R2 must equal R1, fixing the allpass gain at -1.

Design Equations

$$f_0 = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

f_z (frequency of complex zero pair) = f_0

$$Q = \frac{R3}{R2}$$

Q_z (Q of complex zero pair) = $\frac{R3}{R1}$

$$H_{OAP} = -\frac{R2}{R1} = -1$$

$$H_{OLP} = -\left(\frac{R2}{R1} + 1\right) = -2$$

$$H_{OBP} = -\left(1 + \frac{R2}{R1}\right) \times \frac{R3}{R2} = -2\frac{R3}{R2}$$

Circuit Dynamics

$$H_{OBP} = H_{OLP} \times Q = (H_{OAP} + 1)Q$$

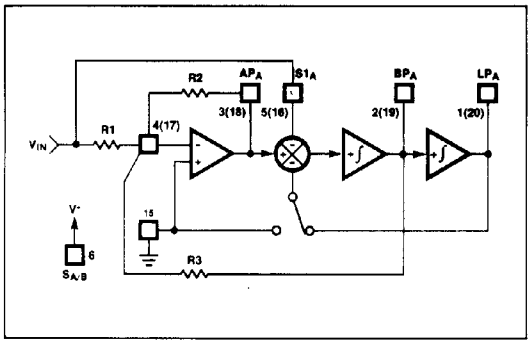


Figure 12. Mode 4

Mode 5
Complex Zero, Bandpass, and Lowpass

The addition of R4 to the circuit of mode 4 allows the independent tuning of the complex zero frequency, f_Z, and the complex pole frequency, f_0. Mode 5 can achieve a more constant allpass amplitude vs. frequency response than can be achieved with mode 4.

Design Equations

$$f_0 = \frac{f_{CLK}}{100} \times \sqrt{1 + \frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{1 + \frac{R2}{R4}}$$

$$f_z = \frac{f_{CLK}}{100} \times \sqrt{1 - \frac{R1}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{1 - \frac{R1}{R4}}$$

$$Q = \frac{R3}{R2} \times \sqrt{1 + \frac{R2}{R4}}$$

$$Q_z = \frac{R3}{R1} \times \sqrt{1 - \frac{R1}{R4}}$$

$$H_{OCZ1} \text{ (as } f \to 0) = \frac{R2(R4 - R1)}{R1(R2 + R4)}$$

$$H_{OCZ2}\left(\text{at } f = \frac{f_{CLK}}{2}\right) = \frac{R2}{R1}$$

$$H_{OBP} = \frac{R3}{R2} \times \left(1 + \frac{R2}{R1}\right)$$

$$H_{OLP} = \frac{R4}{R1} \times \left(\frac{R2 + R1}{R2 + R4}\right)$$

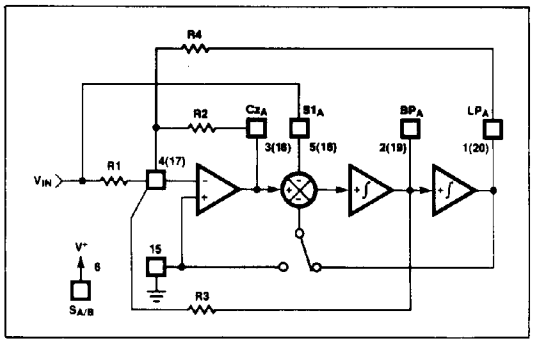


Figure 13. Mode 5

Dual Universal Switched Capacitor Filter

Mode 6A
Single Pole; Highpass and Lowpass

This circuit provides a single real pole for use in odd-ordered cascaded filters. Unlike the simple RC pole used in continuous filters, the MF10 single pole filter can be tuned by simply changing the clock frequency. The cutoff frequency is also resistor tunable.

Design Equations

$$f_c \text{ (cutoff frequency)} = \frac{f_{CLK}}{100} \times \left(\frac{R2}{R3}\right) \text{ or } \frac{f_{CLK}}{50} \times \left(\frac{R2}{R3}\right)$$

$$H_{OLP} = -\frac{R3}{R1}$$

$$H_{OHP} = -\frac{R2}{R1}$$

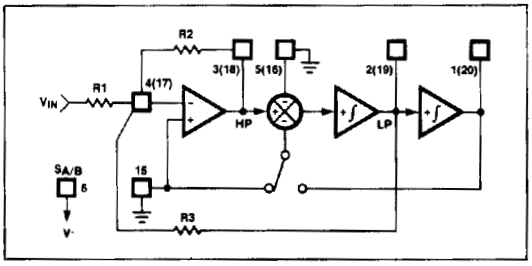


Figure 14. Mode 6A

Mode 6B
Single Lowpass Pole; Inverting and Non-Inverting

As with mode 6A, this mode is useful in implementing filters with an odd number of poles.

Design Equations

$$f_c \text{ (cutoff frequency)} = \frac{f_{CLK}}{100} \times \left(\frac{R2}{R3}\right) \text{ or } \frac{f_{CLK}}{50} \times \left(\frac{R2}{R3}\right)$$

$$H_{OLP} \text{ (inverting output)} = -\frac{R3}{R2}$$

H_{OLP} (non-inverting output) = +1

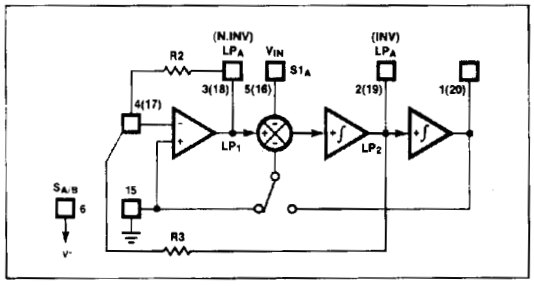


Figure 15. Mode 6B

MF10 Offsets

The MF10's switched capacitor integrators have higher equivalent input offsets than the typical RC integrator in a continuous active filter. The MF10 offsets are produced by parasitic charge injection from the switches into the integrating capacitors. These offsets are relatively independent of clock frequency and temperature. The input offset of the CMOS op amps also contribute to the overall offset error, but these offsets are small in comparison to the offsets caused by charge injection. Figure 16 shows the equivalent circuit for calculating output DC offsets.

V_{OS1} = 0 mV to ±10 mV

V_{OS2} = charge injected offset plus op amp offset
≈ -60 mV to -80 mV (50:1)

V_{OS3} = charge injected offset plus op amp offset
≈ +100 mV to +150 mV (at 50:1)

(At 100:1 the V_{OS2} and V_{OS3} are approximately doubled.)

Using the same designation for resistors as are used in Figures 7 to 15, the output offsets can be calculated as shown below.

Mode 1 and Mode 4 Output Offsets

$$V_{OS(N)} = V_{OS1}\left(\frac{1}{Q} + 1 + |H_{OLP}|\right) - \frac{V_{OS3}}{Q}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

Mode 2 and Mode 5 Output Offsets

$$V_{OS(N)} = \left(\frac{R2}{R_p} \pm 1\right) V_{OS1} \times \frac{1}{1 + R2/R4} + V_{OS2}\frac{1}{1 + R4/R2} - \frac{V_{OS3}}{Q\sqrt{1 + R2/R4}}$$

$$R_p = R1//R2//R4$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

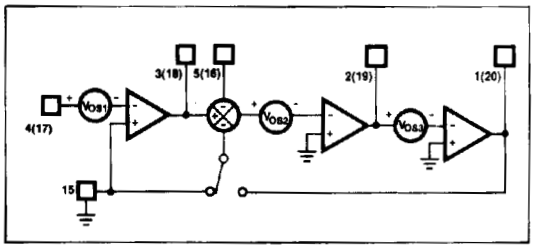


Figure 16. MF10 Offset Model

Mode 3 Output Offsets

$$V_{OS(HP)} = V_{OS2}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = -\frac{R4}{R2} \times \left(\frac{R2}{R3} V_{OS3} + V_{OS2}\right) + \frac{R4}{R2} \times \left(1 + \frac{R2}{R_p}\right) V_{OS1}$$

$$R_p = R1//R3//R4$$

Mode 1A Output Offsets

$$V_{OS(N.INV.BP)} = \left(1 + \frac{1}{Q}\right) V_{OS1} - \frac{V_{OS3}}{Q}$$

$$V_{OS(INV.BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N.INV.BP)} - V_{OS2}$$

In most applications the outputs are AC coupled and the DC offsets present no problem unless large input voltages are applied to the filter.

For Mode 3 operation it should be noted that the use of small R2/R4 ratios and high Q will produce an LP output with a couple of volts DC offset and an offset adjustment should be made. Make the offset adjustment by injecting a small amount of current into the first op amp's inverting input (see Figure 17). This changes V_{OS1} but leaves the output DC offset of the integrators unchanged.

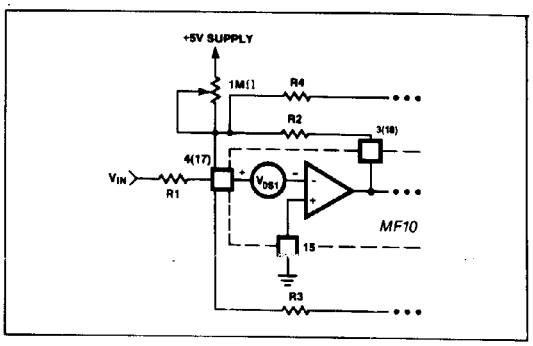


Figure 17. V_{OS} Adjustment

Application Examples

4th Order, 2kHz Lowpass Butterwoth Filter

A 4th order lowpass filter can be made by cascading the two second order filter sections of the MF10 (See Figure 18). Table 3 shows that the two sections of a Butterworth 4th order filter will have the same cutoff frequency, with one stage having a Q of 0.541 and the other stage having a Q of 1.307. Any of the modes may be used, but mode 1A uses only 2 resistors per section, and should therefore be used. The Q of both sections is low, so output clipping will not be a problem.

Using the 2nd order lowpass filter design steps shown in the Filter Design section, the resistor values for the first filter section can be calculated as follows:

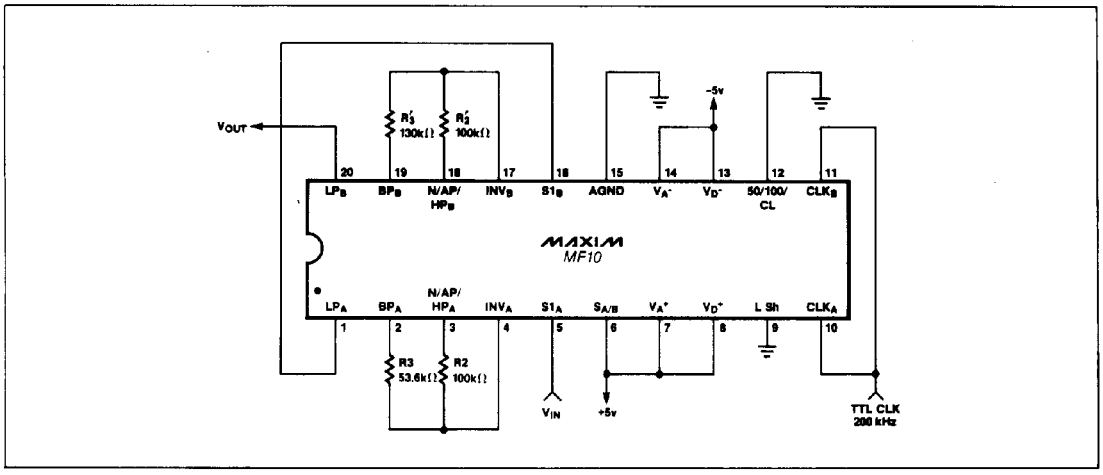


Figure 18. 4th Order, 2kHz Lowpass Butterworth Filter

Dual Universal Switched Capacitor Filter

Mode = 1A

f_0 = 2kHz
Q = 0.541

1) Let R2 be 100kΩ.

2) $f_0 = 2kHz = \frac{f_{CLK}}{100}$ (pin 12 mid-supply)

so f_{CLK} = 200kHz (pin 12 mid-supply)

f_{CLK} = 100kHz with pin 12 high.

3) $Q = \frac{R3}{R2}$;

so R3 = Q x R2 = 0.541 x 100kΩ = 54.1kΩ.

Picking the nearest 1% resistor value, R3 = 53.6 kΩ

Using similar calculations for the second filter section, R2=100kΩ and R3 = 130kΩ.

The output of the first section, LP_A (pin 1), is the input for the second stage, at $S1_B$ (pin 16). The filter output is at LP_B (pin 20). With ±5V supplies and the Level Shift pin connected to ground, the digital input threshold of the CLK inputs is about 1.6V. The CLK inputs can therefore be driven by either TTL or CMOS logic levels. The 50/100/CL pin is grounded, which selects a 100:1 ratio between the clock frequency and the lowpass cutoff frequency.

4th Order Chebyshev Lowpass Filter

Figure 19 shows a 4th order Chebyshev lowpass filter with the following specifications:

Passband Ripple = 2dB (nominal)
Cutoff Frequency = 5kHz

The filter uses a 200kHz clock for both sections.

Table 3 shows that for a 2dB ripple, 4th order Chebyshev filter the parameters of the two sections are:

f_n = 0.471 , Q = 0.929
and
f_n = 0.964 , Q = 4.594

Either mode 3 or mode 2 is suitable for this filter. The resistors for mode 2 can be calculated as follows:

1) Let R2 = 10kΩ.

2) For the first section f_n = 0.471, so for a 5kHz cutoff
f_0 = 0.471 x 5kHz = 2.355kHz

Using the mode 2 equation for f_0,

$$f_0 = \frac{f_{CLK}}{100} \times \sqrt{1 + \frac{R2}{R4}}$$

and using 200kHz for f_{CLK}, R4 is calculated as 25.87kΩ. The closest 1% resistor value of 26.1kΩ is chosen.

3) The mode 2 formula for Q is

$$Q = \frac{R3}{R2} \times \sqrt{1 + \frac{R2}{R4}}$$

Using Q= 0.929 and the previously determined values for R2 and R4, R3 is calculated as 7.9kΩ. The closest 1% value, 7.87kΩ is used.

4) Choose R1 for the desired filter gain. In this example R1 is 10kΩ.

Repeat the above steps for the second section, with f_n = 0.964 and Q = 4.594. If R2 is chosen to be 10kΩ, the value of R4 will be 2.1kΩ and the value of R3 will be 19.1kΩ.

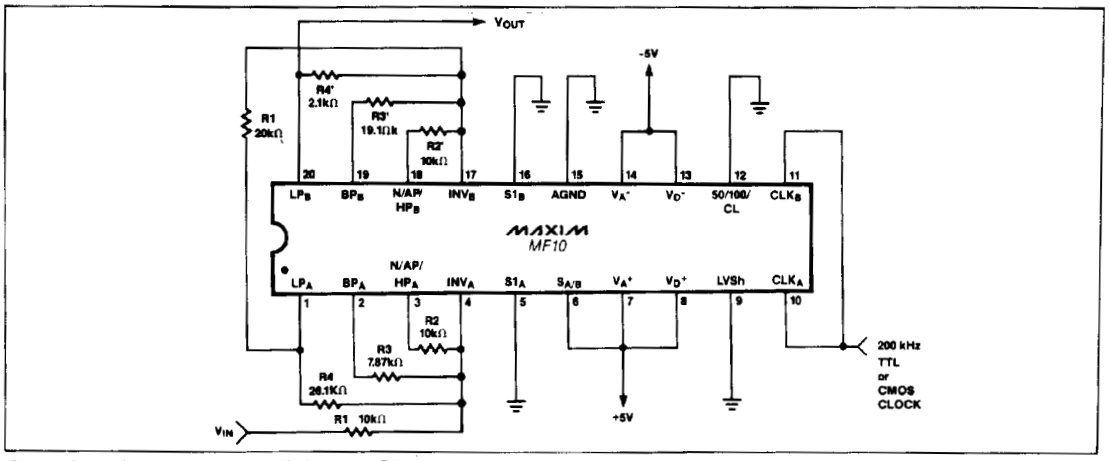


Figure 19. 4th Order Chebyshev 5kHz Lowpass Filter

Switched Capacitor Filter Fundamentals

While it is not necessary to understand the internal operation of the MF10 in order to use it, a basic understanding of switched capacitor operation may help in optimizing designs.

Figure 20 shows a standard integrator using an op amp. The time constant is determined by the passive components, R and C. When a positive input voltage is applied, the integrator output will ramp downward at a rate determined by the input voltage and the time constant, RC. This ramp has a slope of

$$\frac{\Delta V}{\Delta T} = -\frac{V_{IN}}{RC}$$

Figure 21 is a simple inverting switched capacitor integrator, where the R of the standard integrator has been replaced by a capacitor and two analog switches, S1 and S2. As S1 and S2 alternately open and close at the rate set by the clock input, first C1 is charged to the input voltage, then C1 transfers its charge into the capacitor C2. This creates a series of voltage steps on the integrator output, with each voltage step having a value of $-V_{IN}$ x C1/C2. If the value of C1 is small compared to C2, the series of steps at the integrator output approximates a ramp with the slope

$$\frac{\Delta V}{\Delta T} = -\frac{V_{IN} \times f_{CLK} \times C1}{C2}$$

where f_{CLK} is the frequency of the clock input.

This equation is similar to that of the standard integrator, but with the sampled capacitors time constant of

$$\frac{C2}{C1 \times f_{CLK}}$$

replacing the standard integrators time constant of RC. The center frequency of an RC based 2nd order state variable filter is

$$f_0 = \frac{1}{2\pi RC}$$

The center frequency of a switched capacitor 2nd order state variable filter is approximately

$$f_0 = \frac{f_{CLK} \times C1}{2\pi C2}$$

The ratio of C2/C1 in the MF10 is approximately 8 when the 50/100/CL input selects a 50:1 clock to center frequency ratio, and the ratio of C2/C1 is approximately 16 when the 50/100/CL input selects a 100:1 clock to center frequency ratio. Substituting these C2/C1 ratios in the above formula, the MF10 f_0 equation (for modes 1 and 6) results:

$$f_0 = \frac{f_{CLK}}{50} \text{ (50/100/CL Input High)}$$

or

$$f_0 = \frac{f_{CLK}}{100} \text{ (50/100/CL Input Mid-supply)}$$

The integrators used in the MF10 are non-inverting, and use the basic switching scheme of Figure 22. The switches ground one side of the input capacitor C1 when it is connected to the input; and connect the other side to ground while it is connected to the op amp's input. By changing the polarity of C1 in this manner, an additional inversion is added, and overall operation is non-inverting. This means the direction of the voltage ramp at the output of the integrator has the same polarity as V_{IN}.

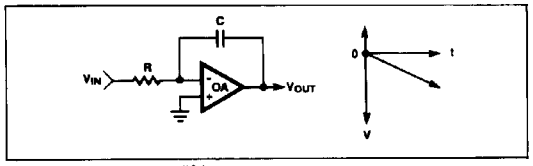


Figure 20. Typical RC integrator

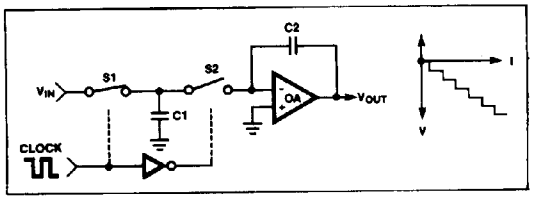


Figure 21. Simple Inverting Switched Capacitor Integrator

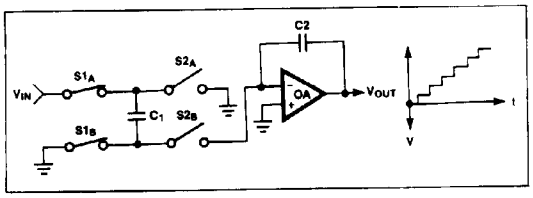
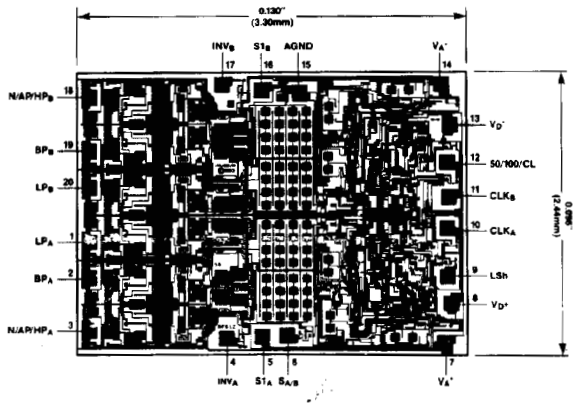


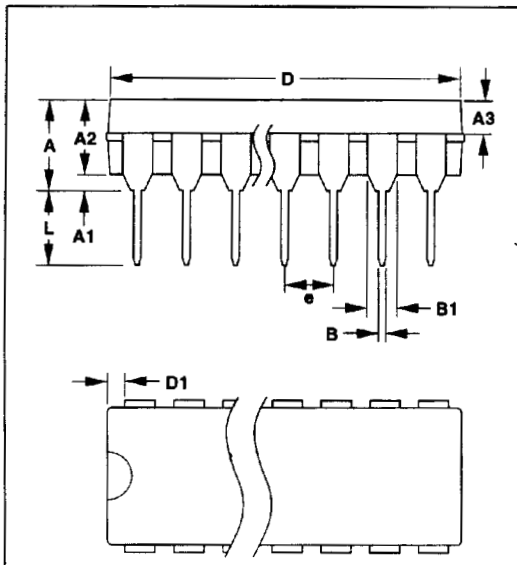
Figure 22. The Non-Inverting Integrator Used in the MF10

Dual Universal Switched Capacitor Filter

Chip Topography



Package Information



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

Plastic DIP PLASTIC DUAL-IN-LINE PACKAGE (0.300 in.)

PKG.	DIM	PINS	INCHES		MILLIMETERS	
			MIN	MAX	MIN	MAX
P	D	8	0.348	0.390	8.84	9.91
P	D	14	0.735	0.765	18.67	19.43
P	D	16	0.745	0.765	18.92	19.43
P	D	18	0.885	0.915	22.48	23.24
P	D	20	1.015	1.045	25.78	26.54
N	D	24	1.14	1.265	28.96	32.13

21-0043A

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