8-BIT N-CHANNEL MICROPROCESSOR

8080
276-2510

GENERAL DESCRIPTION

The INS8080A is an 8-bit microprocessor housed in a standard, 40-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate MOS technology, functions as the central processing unit (CPU) in National Semiconductor's N8080 microcomputer family.

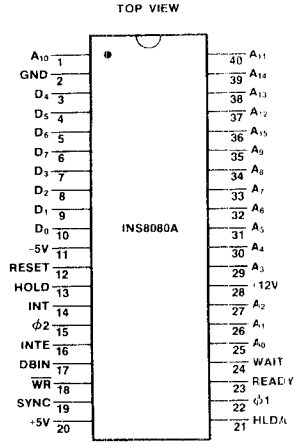
The INS8080A has a 16-bit address bus that is capable of addressing up to 65k bytes of memory and up to 256 input and 256 output devices. Data is routed to and from the INS8080A on a separate bidirectional 8-bit bus. This data bus is also TRI-STATE®, making direct memory addressing (DMA) and multiprocessing applications possible. The INS8080A directly provides signals to control the interface to memory and I/O ports. All buses, including control, are TTL compatible.

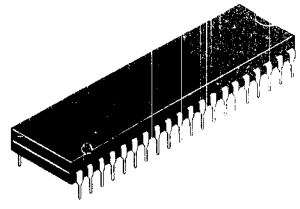
An asynchronous interrupt capability is included in the INS8080A to allow external signals to change the instruction sequence. The interrupting device may vector the program to a particular service routine location (or some other direct function) by specifying an interrupt instruction to be executed.

FEATURES

- 2μs Instruction Cycle
- Variable Length Instructions
- General Purpose Registers—Six plus an Accumulator
- Direct Addressing up to 65k Bytes
- Variable Length Stack Accessed by 16-bit Stack Pointer
- Addresses 256 Input and 256 Output Ports
- Provisions for Vectored Interrupts
- TRI-STATE® Bus for DMA and Multiprocessing Capability
- TRI-STATE TTL Drive Capabilities for Address and Data Buses
- Decimal Arithmetic Capability
- Multiple Addressing Modes
  - —Direct —Register Indirect
  - —Register —Immediate
- Direct Plug-in Replacement for Intel 8080A

PIN CONNECTION





FUNCTIONAL PIN DEFINITION

The following describes the function of all of the INS8080A input/output pins. Some of these descriptions reference internal timing periods.

INPUT SIGNALS

Ready: When high (logic 1), indicates that valid memory or input data are available to the CPU on the INS8080A data bus. The READY signal is used to synchronize the CPU with slower memory or input/output devices. If the INS8080A does not receive a high READY input after sending out an address to memory or an input/output device, the INS8080A enters a WAIT mode for as long as the READY input remains low (logic 0). The CPU may also be single stepped by the use of the READY signal.

Hold: When high, requests that the CPU enter the HOLD mode. When the CPU is in the HOLD mode, the CPU address and data buses both will be in the high-impedance state. The HOLD mode allows an external device to gain control of the INS8080A address and data buses immediately following the completion of the current machine cycle by the CPU. The CPU acknowledges the HOLD mode via the HOLD ACKNOWLEDGE (HLDA) output line. The HOLD request is recognized under the following conditions:

- The CPU is in the HALT mode.
- The READY signal is active and the CPU is in the t_2 or the t_W state.

Interrupt (INT) Request: When high, the CPU recognizes an interrupt request on this line after completing the current instruction or while in the HALT mode. An interrupt request is not honored if the CPU is in the HOLD mode (HLDA = logic 1) or the Interrupt Enable Flip-flop is reset (INTE = logic 0).

Reset: When activated (high) for a minimum of three clock periods, the content of the Program Counter is cleared and the Interrupt Enable and Hold Acknowledge Flip-flops are reset. Following a RESET, program execution starts at memory location 0. It should be noted that the status flags, accumulator, stack pointer, and registers are not cleared during the RESET sequence.

Note: For additional information about the 8080A, refer to Radio Shack's book 62-2014.

Ø1 and Ø2 Clocks: Two non-TTL compatible clock phases which provide nonoverlapping timing references for internal storage elements and logic circuits of the CPU.

+12 Volts: V_{DD} Supply. **+5 Volts:** V_{CC} Supply.
Ground: V_{SS} (0 volt) reference. **-5 Volts:** V_{BB} Supply.

OUTPUT SIGNALS

Synchronizing (SYNC) Signal: When activated (high), the beginning of a new machine cycle is indicated and the status word is outputted on the Data Bus.

Address (A_{15} - A_0) Bus: This bus comprises sixteen TRI-STATE outputlines. The bus provides the address to memory (up to 65k bytes) or denotes the input/output device number for up to 256 input and 256 output peripherals.

Wait: When high, acknowledges that the CPU is in the WAIT mode.

Write (WR): When low, the data on the data bus are stable for WRITE memory or output operation.

Hold Acknowledge (HLDA): Goes high in response to a logic 1 on the HOLD line and indicates that the data and address bus will go to the high-impedance state. The HLDA begins at one of the following times:

- The t_3 state of a READ memory input operation.
- The clock period following the t_3 state of a WRITE memory output operation.

In both cases, the HLDA signal starts after the rising edge of the Ø1 clock, and high impedance occurs after the rising edge of the Ø2 clock.

Interrupt Enable (INTE): Indicates the content of the internal Interrupt Enable Flip-flop. The Enable and Disable Interrupt (EI and DI) Instructions cause the Interrupt Enable Flip-flop to be set and reset, respectively. When the flip-flop is reset (INTE) = logic 0), it inhibits interrupts from being accepted by the CPU. In addition, the Interrupt Enable Flip-flop is automatically reset (thereby disabling further interrupts) at the t_1 state of the instruction fetch cycle, when an interrupt is accepted; it is also reset by the RESET Signal.

Data Bus In (DBIN): When high, indicates to external circuits that the data bus is in the input mode. The DBIN Signal should be used to gate data from memory or an I/O device onto the Data Bus.

INPUT/OUTPUT SIGNALS

Data (D_7 - D_0) Bus: This bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communication between the CPU, memory, and input/output devices for instructions and data transfers. A status word (which describes the current machine cycle) is also outputted on the data bus during the first state of each machine cycle (SYNC = logic 1).

8080A STATUS

Instructions for the 8080A require from one to five machine cycles for complete execution. The 8080A sends out 8 bits of status information on the data bus at the beginning of each machine cycle (during SYNC time). The following table defines the status information.

STATUS INFORMATION DEFINITION

Symbols	Data Bus Bit	Definition
INTA*	D_0	Acknowledge signal for INTERRUPT request Signal should be used to gate a restart instruction onto the data bus when DBIN is active.
WO	D_1	Indicates that the operation in the current machine cycle will be a WRITE memory or OUTPUT function (WO = 0). Otherwise, a READ memory or INPUT operation will be executed.
STACK	D_2	Indicates that the address bus holds the pushdown stack address from the Stack Pointer.
HLTA	D_3	Acknowledge signal for HALT Instruction.
OUT	D_4	Indicates that the address bus contains the address of an output device and the data bus will contain the output data when WR is active.
M_1	D_5	Provides a signal to indicate that the CPU is in the fetch cycle for the first byte of an instruction.
INP*	D_6	Indicates that the address bus contains the address of an input device and the input data should be placed on the data bus when DBIN is active.
MEMR*	D_7	Designates that the data bus will be used for memory read data.

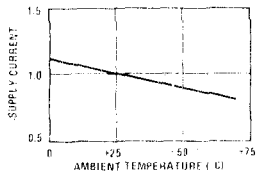
*These three status bits can be used to control the flow of data onto the INS8080A data bus.

CAPACITANCE

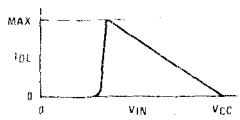
T_A = 25°C, V_{CC} = V_{DD} = V_{SS} = 0V, V_{BB} = -5V

Symbol	Parameter	Typ.	Max.	Unit	Test Condition
$C_\emptyset$	Clock Capacitance	17	25	pF	f_C = 1MHz
C_{IN}	Input Capacitance	6	10	pF	Unmeasured Pins
C_{OUT}	Output Capacitance	10	20	pF	Returned to V_{SS}

Typical Supply Current vs Temperature, Normalized[3]



Data Bus Characteristic During DBIN.



Note 1: The RESET signal must be active for a minimum of 3 clock cycles.
Note 2: When DBIN is high and $V_{IN} > V_{IH}$ an internal active pullup will be switched onto the Data Bus.
Note 3: Δf supply/ ΔT_A = -0.45%/°C.

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	V_{SS}-1	—	V_{SS}+0.8	V	
V_{IHC}	Clock Input High Voltage	9.0	—	V_{DD}+1	V	
V_{IL}	Input Low Voltage	V_{SS}-1	—	V_{SS}+0.8	V	
V_{IH}	Input High Voltage	3.3	—	V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.9mA on all outputs,
V_{OH}	Output High Voltage	3.7			V	I_{OH} = 150µA.
$I_{DD\ AV}$	Avg. Power Supply Current (V_{DD})		40	70	mA	Operation
$I_{CC\ AV}$	Avg. Power Supply Current (V_{CC})		60	80	mA	t_{CY} = 0.48µs
$I_{BB\ AV}$	Avg. Power Supply Current (V_{BB})		0.01	1	mA	
I_{IL}	Input Leakage			±10	µA	$V_{SS} \le V_{IN} \le V_{CC}$
I_{CL}	Clock Leakage			±10	µA	$V_{SS} \le V_{CLOCK} \le V_{DD}$
I_{DL}[2]	Data Bus Leakage in Input Mode			-100 -2.0	µA mA	$V_{SS} \le V_{IN} \le V_{SS}$ + 0.8V V_{SS} + 0.8V $\le V_{IN} \le V_{CC}$
I_{FL}	Address and Data Bus Leakage During HOLD			+10 -100	µA µA	$V_{ADDR\ DATA} = V_{CC}$ $V_{ADDR\ DATA} = V_{SS}$ + 0.45V

STATUS WORD CHART

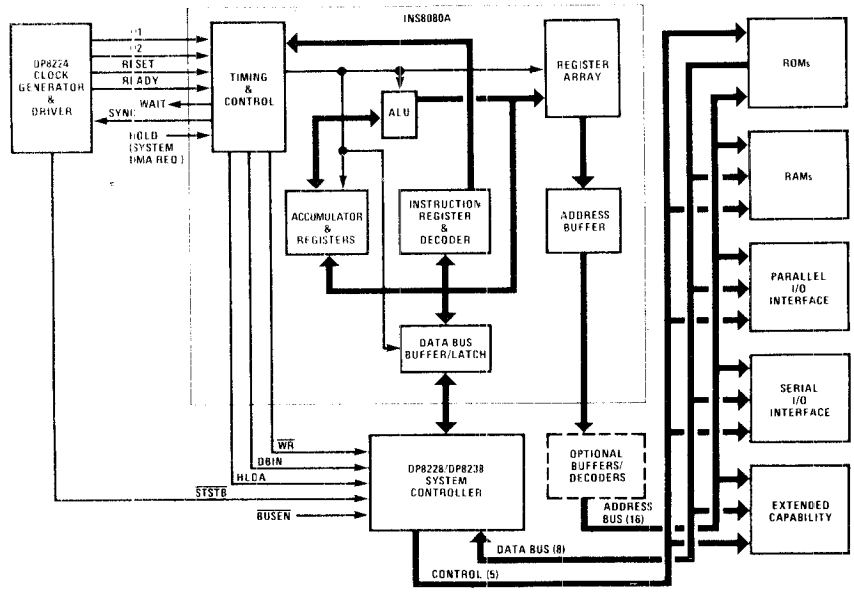
Machine Cycle	Type	Data Bus Bit							
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Instruction Fetch	1	1	0	1	0	0	0	1	0
Memory Read	2	1	0	0	0	0	0	1	0
Memory Write	3	0	0	0	0	0	0	0	0
Stack Read	4	1	0	0	0	0	1	1	0
Stack Write	5	0	0	0	0	0	1	0	0
Input Read	6	0	1	0	0	0	0	1	0
Output Write	7	0	0	0	1	0	0	0	0
Interrupt Acknowledge	8	0	0	1	0	0	0	1	1
Halt Acknowledge	9	1	0	0	0	1	0	1	0
Interrupt Acknowledge While Halt	10	0	0	1	0	1	0	1	1

ABSOLUTE MAXIMUM RATINGS

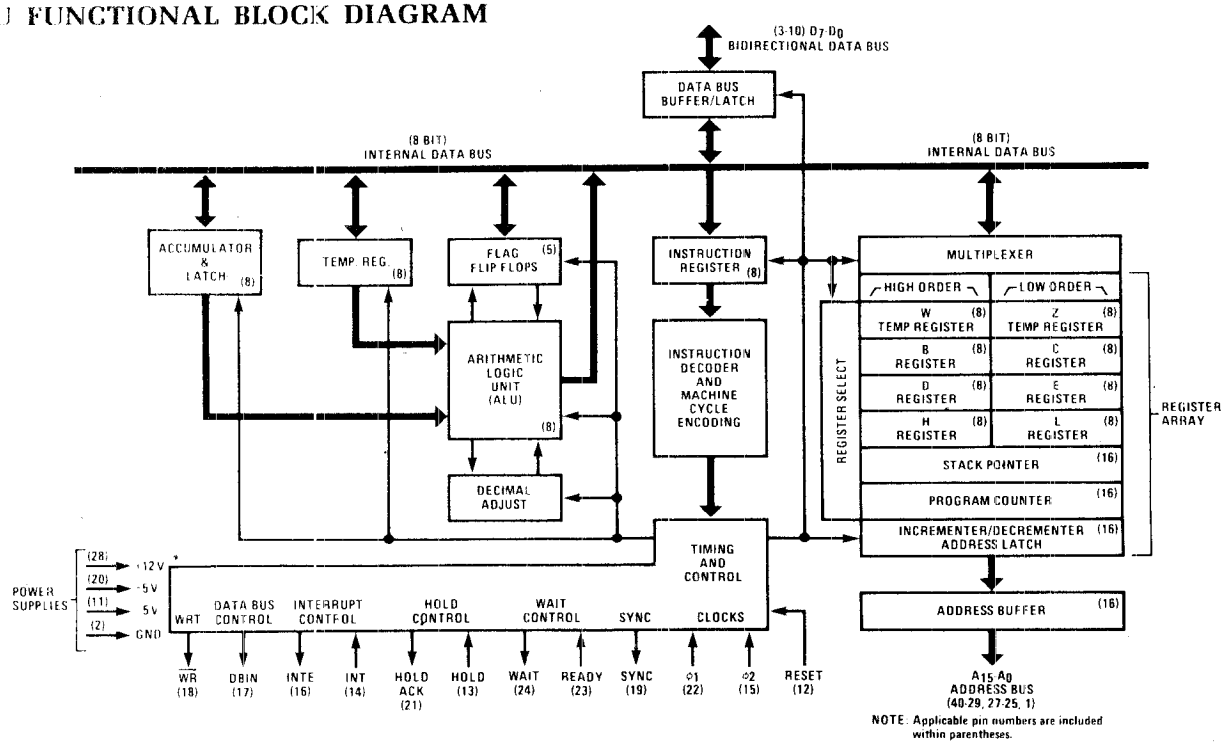
Temperature Under Bias ..... 0°C to +70°C
Storage Temperature ..... -65°C to +150°C
All Input or Output Voltages
with Respect to V_{BB} ..... -0.3V to +20V
V_{CC}, V_{DD} and V_{SS} with Respect to V_{BB} ..... -0.3V to +20V
Power Dissipation 1.5W

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

BLOCK DIAGRAM

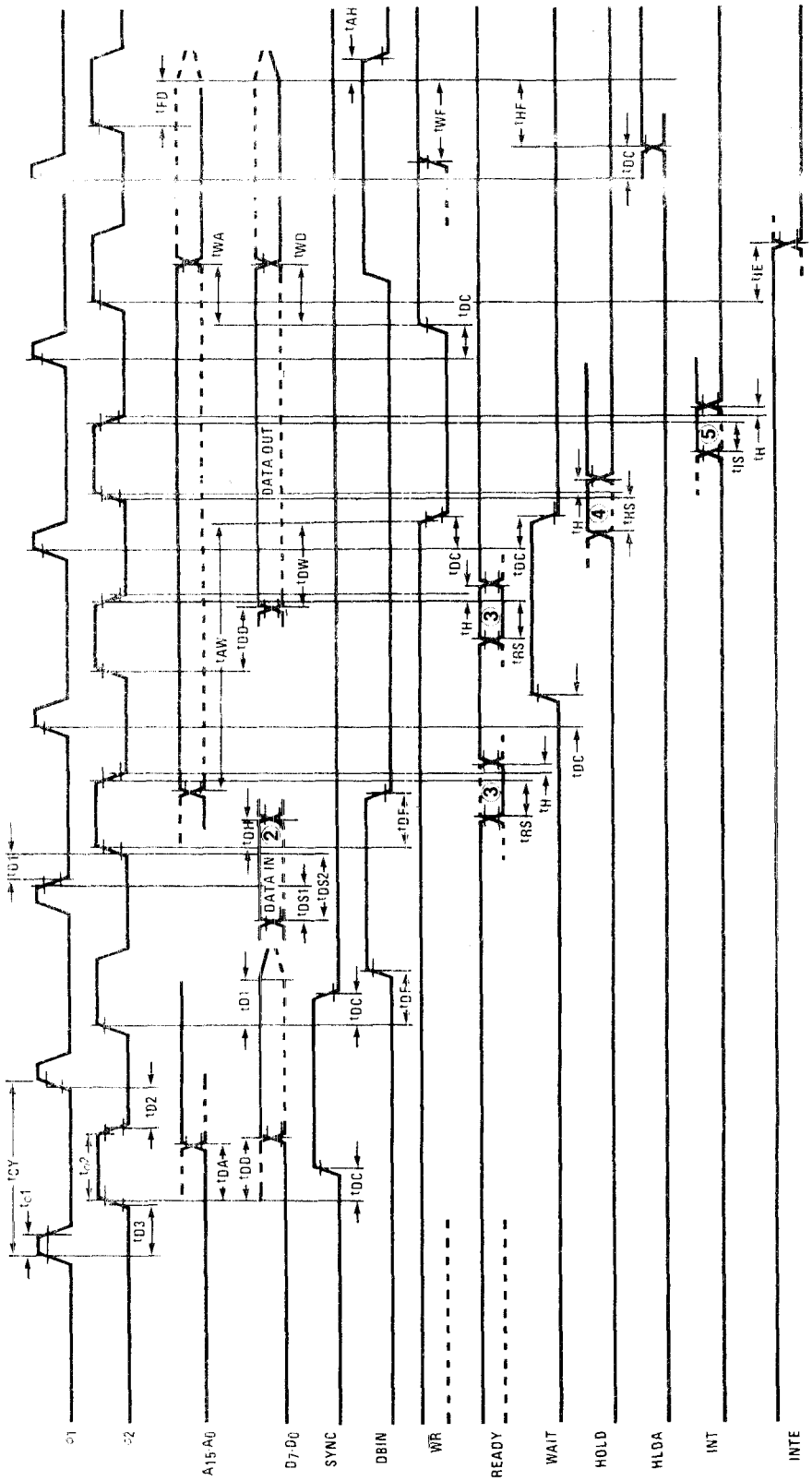


CPU FUNCTIONAL BLOCK DIAGRAM



TIMING WAVEFORMS[1]

Note: Timing measurements are made at the following reference voltages: CLOCK '1' = 8.0V, '0' = 1.0V; INPUTS '1' = 3.3V, '0' = 0.8V; OUTPUTS '1' = 2.0V, '0' = 0.8V.



Note: 1 This timing diagram shows timing relationships only, it does not represent any specific machine cycle.

Note 2: Data in must be stable for this period during DBIN·T_3. Both t_{DS1} and t_{DS2} must be satisfied.

Note 3: Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)

Note 4: Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5 and T_{WH} when in hold mode. (External synchronization is not required.)

Note 5: Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized on the following instruction. (External synchronization is not required.)