i960® RP/RD I/O PROCESSOR AT 3.3 VOLTS

- *33 MHz, 3.3 Volt Version (80960RP 33/3.3)*
- *66 MHz, 3.3 Volt Version (80960RD 66/3.3) - Clock Doubled 80960JF Core*
- *Complies with PCI Local Bus Specification Revision 2.1*
- *5 Volt PCI Signalling Environment*

- **High Performance 80960JF Core**
  - **Sustained One Instruction/Clock Execution**
  - **4 Kbyte Two-Way Set-Associative Instruction Cache**
  - **2 Kbyte Direct-Mapped Data Cache**
  - **Sixteen 32-Bit Global Registers**
  - **Sixteen 32-Bit Local Registers**
  - **Programmable Bus Widths: 8-, 16-, 32-Bit**
  - **1 Kbyte Internal Data RAM**
  - **Local Register Cache (Eight Available Stack Frames)**
  - **Two 32-Bit On-Chip Timer Units**
- **PCI-to-PCI Bridge Unit**
  - **Primary and Secondary PCI Interfaces**
  - **Two 64-Byte Posting Buffers**
  - **Delayed and Posted Transaction Support**
  - **Forwards Memory, I/O, Configuration Commands from PCI Bus to PCI Bus**
- **Two Address Translation Units**
  - **Connects Local Bus to PCI Buses**
  - **Inbound/Outbound Address Translation Support**
  - **Direct Outbound Addressing Support**
- **Messaging Unit**
  - **Four Message Registers**
  - **Two Doorbell Registers**
  - **Four Circular Queues**
  - **1004 Index Registers**
- **Memory Controller**
  - **256 Mbytes of 32- or 36-Bit DRAM**
  - **Interleaved or Non-Interleaved DRAM**
  - **Fast Page-Mode DRAM Support**
  - **Extended Data Out and Burst**
  - **Extended Data Out DRAM Support**
  - **Two Independent Banks for SRAM / ROM / Flash (16 Mbytes/Bank; 8- or 32-Bit)**
- **DMA Controller**
  - **Three Independent Channels**
  - **PCI Memory Controller Interface**
  - **32-Bit Local Bus Addressing**
  - **64-Bit PCI Bus Addressing**
  - **Independent Interface to Primary and Secondary PCI Buses**
  - **132 Mbyte/sec Burst Transfers to PCI and Local Buses**
  - **Direct Addressing to and from PCI Buses**
  - **Unaligned Transfers Supported in Hardware**
  - **Two Channels Dedicated to Primary PCI Bus**
  - **One Channel Dedicated to Secondary PCI Bus**
- **I/O APIC Bus Interface Unit**
  - **Multiprocessor Interrupt Management for Intel Architecture CPUs (Pentium® and Pentium® Pro Processors)**
  - **Dynamic Interrupt Distribution**
  - **Multiple I/O Subsystem Support**
- **I^2C Bus Interface Unit**
  - **Serial Bus**
  - **Master/Slave Capabilities**
  - **System Management Functions**
- **Secondary PCI Arbitration Unit**
  - **Supports Six Secondary PCI Devices**
  - **Multi-priority Arbitration Algorithm**
  - **External Arbitration Support Mode**
- **Private PCI Device Support**
- **SuperBGA* Package**
  - **352 Ball-Grid Array (HL-PBGA)**

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September, 1997 **Order Number:** 273001-002

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1.0 ABOUT THIS DOCUMENT

This is the ADVANCE INFORMATION data sheet for the low-power (3.3 V) versions of Intel's i960® Rx I/O Processor family, including:

- 80960RD 66/3.3
- 80960RP 33/3.3

Throughout this document, these family members are referred to as *80960Rx* when the information is common to both. For product-specific information, such as electrical characteristics, the family member names are used.

This does not contain specifications for the 5 Volt version (80960RP 33/5.0). For specifications on that product, refer to the *i960® RP I/O Processor* Data Sheet (272737).

This data sheet contains a functional overview, mechanical data (package signal locations and simulated thermal characteristics), targeted electrical specifications (simulated), and bus functional waveforms. Detailed functional descriptions other than parametric performance is published in the *i960® RP Microprocessor User's Guide* (272736).

1.1 Solutions960® Program

Intel's *Solutions960®* program features a wide variety of development tools which support the i960 processor family. Many of these tools are developed by partner companies; some are developed by Intel, such as profile-driven optimizing compilers. For more information on these products, contact your local Intel representative.

1.2 Terminology

In this document, the following terms are used:

- *local bus* refers to the 80960Rx's internal local bus, not the PCI local bus.
- *Primary and Secondary PCI buses* are the 80960Rx's internal PCI buses which conform to PCI SIG specifications.
- *80960 core* refers to the 80960JF processor which is integrated into the 80960Rx.

1.3 Additional Information Sources

Intel documentation is available from your local Intel Sales Representative or Intel Literature Sales.

Intel Corporation
Literature Sales
P.O. Box 7641
Mt. Prospect IL 60056-7641
1-800-879-4683

Table 1. Related Documentation

Document Title	Order / Contact
i960® RP Microprocessor User's Guide	Intel Order # 272736
i960® RP Processor: A Single-Chip Intelligent I/O Subsystem Technical Brief	Intel Order # 272738
i960® Jx Microprocessor User's Guide	Intel Order # 272483
80960RP Specification Update	Intel Order # 272918
PCI Local Bus Specification Revision 2.1	PCI Special Interest Group 1-800-433-5177
PCI-to-PCI Bridge Architecture Specification Revision 1.0	PCI Special Interest Group 1-800-433-5177
I^2C Peripherals for Microcontrollers	Philips Semiconductor

2.0 FUNCTIONAL OVERVIEW

As indicated in Figure 1, the 80960Rx combines many features with the 80960JF to create an intelligent I/O processor. Subsections following the figure briefly describe the main features; for detailed functional descriptions, refer to the *i960® RP Microprocessor User's Guide* (272736).

The PCI bus is an industry standard, high performance, low latency system bus that operates up to 132 Mbyte/s. The 80960Rx, a multi-function PCI device, is fully compliant with the *PCI Local Bus Specification* Revision 2.1. Function 0 is the PCI-to-PCI bridge unit; Function 1 is the address translation unit.

The PCI-to-PCI bridge unit is the connection path between two independent 32-bit PCI buses and provides the ability to overcome PCI electrical load limits. The addition of the i960 core processor brings intelligence to the bridge.

The 80960Rx, object code compatible with the i960 core processor, is capable of sustained execution at the rate of one instruction per clock.

The local bus, a 32-bit multiplexed burst bus, is a high-speed interface to system memory and I/O. A full complement of control signals simplifies the connection of the 80960Rx to external components. Physical and logical memory attributes are programmed via memory-mapped control registers (MMRs), an extension not found on the i960 Kx, Sx or Cx processors. Physical and logical configuration registers enable the processor to operate with all combinations of bus width and data object alignment.

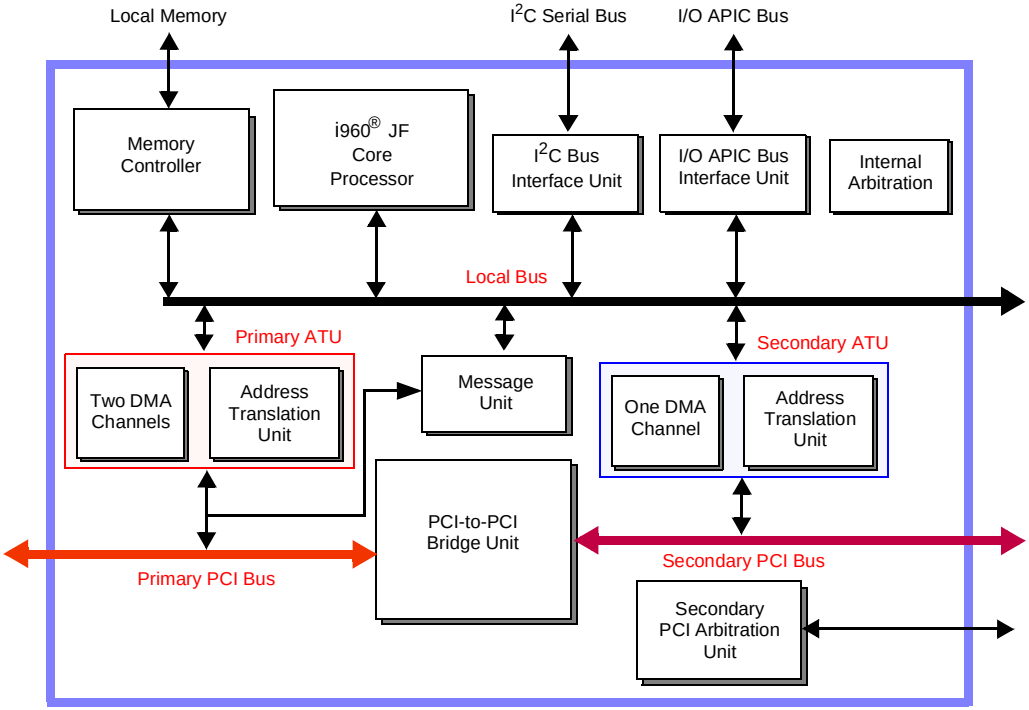


Figure 1. i960® Rx I/O Processor at 3.3 V Functional Block Diagram

2.1 Key Functional Units

2.1.1 PCI-to-PCI Bridge Unit

The PCI-to-PCI bridge unit (referred to as “bridge”) connects two independent PCI buses. It is fully compliant with the *PCI-to-PCI Bridge Architecture Specification* Revision 1.0 published by the PCI Special Interest Group. It allows certain bus transactions on one PCI bus to be forwarded to the other PCI bus. Dedicated data queues support high performance bandwidth on the PCI buses. The i960® Rx I/O Processor at 3.3 V supports PCI 64-bit Dual Address Cycle (DAC) addressing.

The bridge has dedicated PCI configuration space that is accessible through the primary PCI bus.

2.1.2 Private PCI Device Support

A key design feature is that the 80960Rx explicitly supports private PCI devices on the secondary PCI bus without being detected by PCI configuration software. The bridge and Address Translation Unit work together to hide private devices from PCI configuration cycles and allow these devices to use a private PCI address space. The Address Translation Unit uses normal PCI configuration cycles to configure these devices.

2.1.3 DMA Controller

The DMA Controller supports low-latency, high-throughput data transfers between PCI bus agents and 80960 local memory. Three separate DMA channels accommodate data transfers: two for primary PCI bus, one for the secondary PCI bus. The DMA Controller supports chaining and unaligned data transfers. It is programmable only through the i960 core processor.

2.1.4 Address Translation Unit

The Address Translation Unit (ATU) allows PCI transactions direct access to the 80960Rx local memory. The 80960Rx has direct access to both PCI buses. The ATU supports transactions between PCI address space and 80960Rx address space.

Address translation is controlled through programmable registers accessible from both the PCI interface and the 80960 core. Dual access to registers allows flexibility in mapping the two address spaces.

2.1.5 Messaging Unit

The Messaging Unit (MU) provides data transfer between the PCI system and the 80960Rx. It uses interrupts to notify each system when new data arrives. The MU has four messaging mechanisms. Each allows a host processor or external PCI device and the 80960Rx to communicate through message passing and interrupt generation. The four mechanisms are Message Registers, Doorbell Registers, Circular Queues, and Index Registers.

2.1.6 Memory Controller

The Memory Controller allows direct control of external memory systems, including DRAM, SRAM, ROM and Flash Memory. It provides a direct connect interface to memory that typically does not require external logic. It features programmable chip selects, a wait state generator and byte parity. External memory can be configured as PCI addressable memory or private processor memory.

2.1.7 I^2C Bus Interface Unit

The I^2C (Inter-Integrated Circuit) Bus Interface Unit allows the 80960 core to serve as a master and slave device residing on the I^2C bus. The I^2C bus is a serial bus developed by Philips Semiconductor consisting of a two pin interface. The bus allows the 80960Rx to interface to other I^2C peripherals and microcontrollers for system management functions. It requires a minimum of hardware for an economical system to relay status and reliability information on the I/O subsystem to an external device. For more information, see *I^2C Peripherals for Microcontrollers* (Philips Semiconductor)

2.1.8 I/O APIC Bus Interface Unit

The I/O APIC Bus Interface Unit provides an interface to the three-wire Advanced Programmable Interrupt Controller (APIC) bus that allows I/O APIC emulation in software. Interrupt messages can be sent on the bus and EOI messages can be received.

2.1.9 Secondary PCI Arbitration Unit

The Secondary PCI Arbitration Unit provides PCI arbitration for the secondary PCI bus. It includes a fairness algorithm with programmable priorities and six PCI Request and Grant signal pairs. This arbitration unit can also be disabled to allow for external arbitration.

2.2 i960 Core Features (80960JF)

The processing power of the 80960Rx comes from the 80960JF processor core. The 80960JF is a new, scalar implementation of the 80960 Core Architecture. Figure 2 shows a block diagram of the 80960JF Core processor.

Factors that contribute to the 80960 family core's performance include:

- Single-clock execution of most instructions
- Independent Multiply/Divide Unit
- Efficient instruction pipeline minimizes pipeline break latency
- Register and resource scoreboarding allow overlapped instruction execution
- 128-bit register bus speeds local register caching
- 4 Kbyte two-way set-associative, integrated instruction cache
- 2 Kbyte direct-mapped, integrated data cache
- 1 Kbyte integrated data RAM delivers zero wait state program data

The 80960 core operates out of its own 32-bit address space, which is independent of the PCI address space. The local bus memory can be:

- Made visible to the PCI address space
- Kept private to the 80960 core
- Allocated as a combination of the two

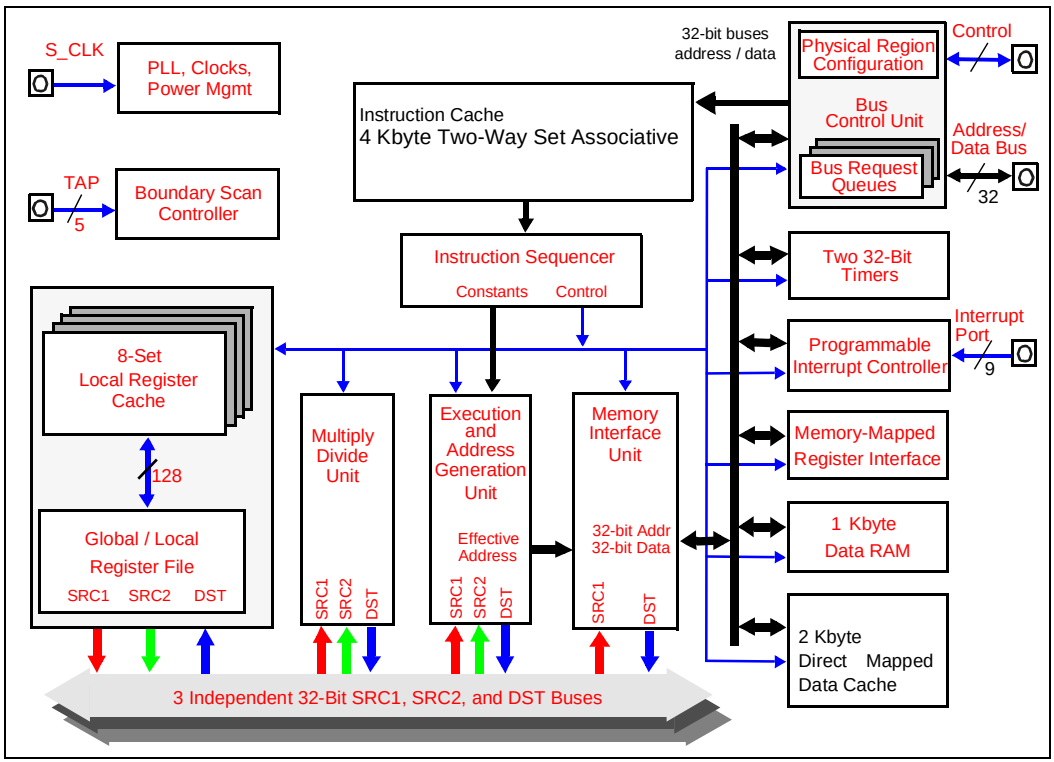


Figure 2. 80960JF Core Block Diagram

2.2.1 Burst Bus

A 32-bit high-performance bus controller interfaces the 80960Rx to external memory and peripherals. The Bus Control Unit fetches instructions and transfers data on the local bus at the rate of up to four 32-bit words per six clock cycles. The external address/data bus is multiplexed.

Users may configure the 80960Rx's bus controller to match an application's fundamental memory organization. Physical bus width is programmable for up to eight regions. Data caching is programmed through a group of logical memory templates and a defaults register. The Bus Control Unit's features include:

- Multiplexed external bus minimizes pin count
- 32-, 16- and 8-bit bus widths simplify I/O interfaces
- External ready control for address-to-data, data-to-data and data-to-next-address wait state types
- Little endian byte ordering
- Unaligned bus accesses performed transparently
- Three-deep load/store queue decouples the bus from the 80960 core

Upon reset, the 80960Rx conducts an internal self test. Before executing its first instruction, it performs an external bus confidence test by performing a checksum on the first words of the Initialization Boot Record.

2.2.2 Timer Unit

The timer unit (TU) contains two independent 32-bit timers that are capable of counting at several clock rates and generating interrupts. Each is programmed by use of the Timer Unit registers. These memory-mapped registers are addressable on 32-bit boundaries. The timers have a single-shot mode and auto-reload capabilities for continuous operation. Each timer has an independent interrupt request to the 80960Rx's interrupt controller. The TU can generate a fault when unauthorized writes from user mode are detected.

2.2.3 Priority Interrupt Controller

Low interrupt latency is critical to many embedded applications. As part of its highly flexible interrupt mechanism, the 80960Rx exploits several techniques to minimize latency:

- Interrupt vectors and interrupt handler routines can be reserved on-chip
- Register frames for high-priority interrupt handlers can be cached on-chip
- The interrupt stack can be placed in cacheable memory space

2.2.4 Faults and Debugging

The 80960Rx employs a comprehensive fault model. The processor responds to faults by making implicit calls to a fault handling routine. Specific information collected for each fault allows the fault handler to diagnose exceptions and recover appropriately.

The processor also has built-in debug capabilities. Via software, the 80960Rx may be configured to detect as many as seven different trace event types. Alternatively, **mark** and **fmark** instructions can generate trace events explicitly in the instruction stream. Hardware breakpoint registers are also available to trap on execution and data addresses.

2.2.5 On-Chip Cache and Data RAM

Memory subsystems often impose substantial wait state penalties. The 80960Rx integrates considerable storage resources on-chip to decouple CPU execution from the external bus. It also includes a 4 Kbyte instruction cache, a 2 Kbyte data cache and 1 Kbyte data RAM.

2.2.6 Local Register Cache

The 80960Rx rapidly allocates and deallocates local register sets during context switches. The processor needs to flush a register set to the stack only when it saves more than seven sets to its local register cache.

2.2.7 Test Features

The 80960Rx incorporates numerous features that enhance the user's ability to test both the processor and the system to which it is attached. These features include ONCE (On-Circuit Emulation) mode and Boundary Scan (JTAG).

The 80960Rx provides testability features compatible with IEEE Standard Test Access Port and Boundary Scan Architecture (IEEE Std. 1149.1).

One of the boundary scan instructions, HIGHZ, forces the processor to float all its output pins (ONCE mode). ONCE mode can also be initiated at reset without using the boundary scan mechanism.

ONCE mode is useful for board-level testing. This feature allows a mounted 80960Rx to electrically “remove” itself from a circuit board. This mode allows system-level testing where a remote tester can exercise the processor system.

The test logic does not interfere with component or system behavior and ensures that components function correctly, and also the connections between various components are correct.

The JTAG Boundary Scan feature is an alternative to conventional “bed-of-nails” testing. It can examine connections that might otherwise be inaccessible to a test system.

2.2.8 Memory-Mapped Control Registers

The 80960Rx is compliant with 80960 family architecture and has the added advantage of memory-mapped, internal control registers not found on the 80960Kx, Sx or Cx processors. This feature provides software an interface to easily read and modify internal control registers.

Each memory-mapped, 32-bit register is accessed via regular memory-format instructions. The processor ensures that these accesses do not generate external bus cycles.

2.2.9 Instructions, Data Types and Memory Addressing Modes

As with all 80960 family processors, the 80960Rx instruction set supports several different data types and formats:

- Bit
- Bit fields
- Integer (8-, 16-, 32-, 64-bit)
- Ordinal (8-, 16-, 32-, 64-bit unsigned integers)
- Triple word (96 bits)
- Quad word (128 bits)

The 80960Rx provides a full set of addressing modes for C and assembly:

- Two Absolute modes
- Five Register Indirect modes
- Index with displacement mode
- IP with displacement mode

Table 2 shows the available instructions.

Table 2. 80960Rx Instruction Set

Data Movement	Arithmetic	Logical	Bit, Bit Field and Byte
Load	Add	And	Set Bit
Store	Subtract	Not And	Clear Bit
Move	Multiply	And Not	Not Bit
Conditional Select	Divide	Or	Alter Bit
Load Address	Remainder	Exclusive Or	Scan For Bit
	Modulo	Not Or	Span Over Bit
	Shift	Or Not	Extract
	Extended Shift	Nor	Modify
	Extended Multiply	Exclusive Nor	Scan Byte for Equal
	Extended Divide	Not	Byte Swap
	Add with Carry	Nand	
	Subtract with Carry		
	Conditional Add		
	Conditional Subtract		
	Rotate		
Comparison	**Branch**	**Call/Return**	**Fault**
Compare	Unconditional Branch	Call	Conditional Fault
Conditional Compare	Conditional Branch	Call Extended	Synchronize Faults
Compare and Increment	Compare and Branch	Call System	
Compare and Decrement		Return	
Test Condition Code		Branch and Link	
Check Bit			
Debug	**Processor Management**	**Atomic**	
Modify Trace Controls	Flush Local Registers	Atomic Add	
Mark	Modify Arithmetic Controls	Atomic Modify	
Force Mark	Modify Process Controls		
	Halt		
	System Control		
	Cache Control		
	Interrupt Control		

3.0 PACKAGE INFORMATION

3.1 Package Introduction

The 80960Rx is offered in a SuperBGA* Ball Grid Array (HL-PBGA) package. This is a perimeter array package with four rows of ball connections in the outer area of the package. See Figure 4, 352L HL-PBGA Package Diagram (Bottom View) (pg. 22).

Section 3.1.1, Functional Signal Definitions describes signal function; **Section 3.1.2, 352-Lead HL-PBGA Package** defines the signal and ball locations.

3.1.1 Functional Signal Definitions

Table 3 presents the legend for interpreting the Type Field in the following tables. Table 4 defines signals associated with the bus interface. Table 5 defines signals associated with basic control and test functions. Table 6 defines signals associated with the Interrupt Unit. Table 7 defines PCI signals. Table 8 defines Memory Controller signals. Table 9 defines DMA, APIC and I^2C signals. Table 10 defines clock signals. Table 11 defines ICE signals.

Table 3. Signal Type Definition

Symbol	Description
I	Input signal only.
O	Output signal only.
I/O	Signal can be either an input or output.
OD	Open Drain signal.
–	Signal must be connected as described.
S (...)	Synchronous. Inputs must meet setup and hold times relative to S_CLK. S(E) Edge sensitive input S(L) Level sensitive input
A (...)	Asynchronous. Inputs may be asynchronous relative to S_CLK. A(E) Edge sensitive input A(L) Level sensitive input
R (...)	While the P_RST# signal is asserted, the signal: R(1) is driven to V_{CC} R(0) is driven to V_{SS} R(Q) is a valid output R(Z) Floats R(H) is pulled up to V_{CC} R(X) is driven to an unknown state
H (...)	While the 80960Rx is in the hold state, the signal: H(1) is driven to V_{CC} H(0) is driven to V_{SS} H(Q) Maintains previous state or continues to be a valid output H(Z) Floats
P (...)	While the 80960Rx is halted, the signal: P(1) is driven to V_{CC} P(0) is driven to V_{SS} P(Q) Maintains previous state or continues to be a valid output
K (...)	While the Secondary PCI Bus is being parked, the signal: K(Z) Floats K(Q) Maintains previous state or continues to be a valid output

Table 4. Signal Descriptions (Sheet 1 of 5)

NAME	TYPE	DESCRIPTION
AD31:0	**I/O** S(L) R(Z) H(Z) P(Q)	**ADDRESS / DATA BUS** carries 32-bit physical addresses and 8-, 16- or 32-bit data to and from memory. During an address (T_a) cycle, bits 2-31 contain a physical word address (bits 0-1 indicate SIZE; see below). During a data (T_d) cycle, read or write data is present on one or more contiguous bytes, comprising AD31:24, AD23:16, AD15:8 and AD7:0. During write operations, unused signals are driven to determinate values. **SIZE**, which comprises bits 0-1 of the AD lines during a T_a cycle, specifies the number of data transfers during the bus transaction on the local bus. When the DMA or ATUs initiate data transfers, transfer size shown below is **not** valid. **AD1 AD0 Bus Transfers** 0 0 1 Transfer 0 1 2 Transfers 1 0 3 Transfers 1 1 4 Transfers When the 80960Rx enters Halt mode and the previous bus operation was: • write — AD31:2 are driven with the last data value on the AD bus. • read — AD31:2 are driven with the last address value on the AD bus. Typically, AD1:0 reflect the SIZE information of the last bus transaction (either instruction fetch or load/store) that was executed before entering Halt mode.
ADS#	**O** R(1) H(Z) P(1)	**ADDRESS STROBE** indicates a valid address and the start of a new bus access. The processor asserts ADS# for the entire T_a cycle. External bus control logic typically samples ADS# at the end of the cycle.
ALE	**O** R(0) H(Z) P(0)	**ADDRESS LATCH ENABLE** indicates the transfer of a physical address. ALE is asserted during a T_a cycle and deasserted before the beginning of the T_d state. It is active HIGH and floats to a high impedance state during a hold cycle (T_h).
BLAST#	**O** H(Z) P(1)	**BURST LAST** indicates the last transfer in a bus access. BLAST# is asserted in the last data transfer of burst and non-burst accesses. BLAST# remains active while wait states are detected via the LRDYRCV# or RDYRCV# signal on the memory controller. BLAST# becomes inactive after the final data transfer in a bus cycle. BLAST# has a weak internal pullup which is active during reset to ensure normal operation when the signal is not connected. 0 = Last Data Transfer 1 = Not the Last Data Transfer

Table 4. Signal Descriptions (Sheet 2 of 5)

NAME	TYPE	DESCRIPTION
BE3:0#	**O** R(1) H(Z) P(1)	**BYTE ENABLES** select which of up to four data bytes on the bus participate in the current bus access. Byte enable encoding depends on the bus width of the memory region accessed: *32-bit bus:* BE3# enables data on AD31:24 BE2# enables data on AD23:16 BE1# enables data on AD15:8 BE0# enables data on AD7:0 *16-bit bus:* BE3# becomes Byte High Enable (enables data on AD15:8) BE2# is not used (state is high) BE1# becomes Address Bit 1 (A1) (increments with the assertion of LRDY# or RDYRCV#) BE0# becomes Byte Low Enable (enables data on AD7:0) *8-bit bus:* BE3# is not used (state is high) BE2# is not used (state is high) BE1# becomes Address Bit 1 (A1) (increments with the assertion of LRDY# or RDYRCV#) BE0# becomes Address Bit 0 (A0) (increments with the assertion of LRDY# or RDYRCV#) The processor asserts byte enables, byte high enable and byte low enable during T_a. Since unaligned bus requests are split into separate bus transactions, these signals do not toggle during a burst (32-bit bus only) from the i960 core processor; they do toggle for DMA and ATU cycles. They remain active through the last T_d cycle.
DEN#	**O** H(Z) P(1)	**DATA ENABLE** indicates data transfer cycles during a bus access. DEN# is asserted at the start of the first data cycle in a bus access and deasserted at the end of the last data cycle. DEN# is used with DT/R# to provide control for data transceivers connected to the data bus. DEN# has a weak internal pullup which is active during reset to ensure normal operation when the signal is not connected. 0 = Data Cycle 1 = Not a Data Cycle

Table 4. Signal Descriptions (Sheet 3 of 5)

NAME	TYPE	DESCRIPTION
D/C#/ RST_MODE#	**I/O** R(H) H(Z) P(Q)	**DATA/CODE/RESET_MODE** indicates that a bus access is a data access or an instruction access. D/C# has the same timing as W/R#. 0 = Instruction Access 1 = Data Access The RST_MODE# signal is sampled at Primary PCI bus reset to determine whether the 80960 core is to be held in reset. When RST_MODE# is high, the 80960Rx begins initialization immediately following the deassertion of P_RST. When RST_MODE is low, the 80960 core remains in reset until the 80960 core reset bit is cleared in the extended bridge control register. This signal has a weak internal pullup that is active during reset to ensure normal operation when the signal is left unconnected. 0 = RST_MODE enabled 1 = RST_MODE not enabled While the 80960 core is in reset, all peripherals may be accessed from the primary or secondary PCI buses depending on the status of the WIDTH/HLTD1/RETRY/ signal.
DT/R#	**O** R(0) H(Z) P(Q)	**DATA TRANSMIT / RECEIVE** indicates the direction of data transfer to and from the address/data bus. It is low during T_a and T_w/T_d cycles for a read; it is high during T_a and T_w/T_d cycles for a write. DT/R# never changes state when DEN# is asserted. 0 = Receive 1 = Transmit
LOCK#/ONCE#	**I/O** S(L) R(H) H(Z) P(Q)	**BUS LOCK** indicates that an atomic read-modify-write operation is in progress. The LOCK# output is asserted in the first clock of an atomic operation and deasserted in the last data transfer of the sequence. The processor does not grant HOLDA while asserting LOCK#. This prevents external agents from accessing memory involved in semaphore operations. 0 = Atomic Read-Modify-Write in Progress 1 = No Atomic Read-Modify-Write in Progress **ONCE MODE:** The processor samples the ONCE input during reset. When ONCE# is asserted LOW at the end of reset, the processor enters ONCE mode, stops all clocks and floats all output signals. LOCK#/ONCE# has a weak internal pullup which is active during reset to ensure normal operation when the signal is not connected. 0 = ONCE Mode Enabled 1 = ONCE Mode Not Enabled
LRDYRCV#	**O** R(1) H(Q) P(Q)	**LOCAL READY/RECOVER**, generated by the 80960Rx's memory controller unit, is an output version of the READY/RECOVER (RDYRCV#) signal. Refer to the RDYRCV# signal description.

Table 4. Signal Descriptions (Sheet 4 of 5)

NAME	TYPE	DESCRIPTION
HOLD	**I** S(L)	HOLD is a request from an external bus master to acquire the bus. When the processor receives HOLD and grants bus control to another master, it asserts HOLDA, floats the address/data and control lines and enters the T_h state. When HOLD is deasserted, the processor deasserts HOLDA and enters either the T_i or T_a state, resuming control of the address/data and control lines. See Figure 32, HOLD/HOLDA Waveform For Bus Arbitration (pg. 61). 0 = No Hold Request 1 = Hold Requested
HOLDA	**O** R(0) H(1) P(Q)	**HOLD ACKNOWLEDGE** indicates to an external bus master that the processor has relinquished bus control. The processor can grant HOLD requests and enter the T_h state and while halted as well as during regular operation. See Figure 32, HOLD/HOLDA Waveform For Bus Arbitration (pg. 61). 0 = No Hold Acknowledged 1 = Hold Acknowledged
RDYRCV#	**I** S(L)	**READY/RECOVER** is only used in systems that use an external memory controller (and do not use the 80960Rx's memory controller unit). This signal indicates that data on AD lines can be sampled or removed. When RDYRCV# is not asserted during a T_d cycle, the T_d cycle extends to the next cycle by inserting a wait state (T_w). 0 = Sample Data 1 = Do Not Sample Data RDYRCV# has an alternate function during the recovery (T_r) state. The processor continues to insert recovery states until it samples the signal HIGH. This gives slow external devices more time to float their buffers before the processor drives addresses. 0 = Insert Wait States 1 = Recovery Complete When using the internal memory controller, connect this signal to V_{CC} through a 2.7 KΩ resistor.
W/R#	**O** R(0) H(Z) P(Q)	**WRITE/READ** specifies during a T_a cycle whether the operation is a write or read. It is latched on-chip and remains valid during T_d cycles. 0 = Read 1 = Write
WIDTH/ HLTD0	**I/O** R(H) H(Z) P(Q)	**WIDTH** denotes the physical memory attributes for a bus transaction in conjunction with WIDTH/HLTD1/RETRY: WIDTH/HLTD1/RETRY — WIDTH/HLTD0 0 — 0 — 8 Bits Wide 0 — 1 — 16 Bits Wide 1 — 0 — 32 Bits Wide 1 — 1 — Undefined **WIDTH/HLTD0** For proper operation, do not connect this signal to ground. This signal has a weak internal pullup which is active during reset to ensure normal operation. **HLTD0** signal name has no function in the 80960Rx; the signal name is included for 80960JF naming convention compatibility.

Table 4. Signal Descriptions (Sheet 5 of 5)

NAME	TYPE	DESCRIPTION
WIDTH/ HLTD1/ RETRY	**I/O** R(H) H(Z) P(Q)	**WIDTH** denotes the physical memory attributes for a bus transaction in conjunction with the WIDTH/HLTD0 signal. Refer to description above. RETRY is sampled at Primary PCI bus reset to determine when the Primary PCI interface is disabled. When high, the Primary PCI interface disables PCI configuration cycles by signaling a RETRY until the Extended Bridge Control Register's Configuration Cycle Disable bit is cleared. When low, the Primary PCI interface allows configuration cycles to occur. WIDTH/HLTD1/RETRY has a weak internal pullup which is active during reset to ensure normal operation when the signal is not connected. HLTD1 signal name has no function in the 80960Rx; the signal name is included for 80960JF naming convention compatibility.

Table 5. Power Requirement, Processor Control and Test Signal Descriptions (Sheet 1 of 2)

NAME	TYPE	DESCRIPTION
FAIL#	**O** R(0) H(Q)	**FAIL** indicates a failure of the processor's built-in self-test performed during initialization. FAIL# is asserted immediately upon reset and toggles during self-test to indicate the status of individual tests: • When self-test passes, the processor deasserts FAIL# and commences operation from user code. • When self-test fails, the processor asserts FAIL# and then stops executing. Self-test failing does not cause the bridge to stop execution. 0 = Self Test Failed 1 = Self Test Passed
L_RST#	**O**	**LOCAL BUS RESET** notifies external devices that the local bus has reset.
STEST	**I** S(L)	**SELF TEST** enables or disables the processor's internal self-test feature at initialization. STEST is examined at the end of P_RST#. When STEST is asserted, the processor performs its internal self-test and the external bus confidence test. When STEST is deasserted, the processor performs only the external bus confidence test. 0 = Self Test Disabled 1 = Self Test Enabled
TCK	**I**	**TEST CLOCK** is a CPU input that provides the clocking function for IEEE 1149.1 Boundary Scan Testing (JTAG). State information and data are clocked into the processor on the rising edge; data is clocked out of the processor on the falling edge.
TDI	**I** S(L)	**TEST DATA INPUT** is the serial input signal for JTAG. TDI is sampled on the rising edge of TCK, during the SHIFT-IR and SHIFT-DR states of the Test Access Port. This signal has a weak internal pullup which is active during reset to ensure normal operation when the signal is not connected.
TDO	**O** R(Q) H(Q) P(Q)	**TEST DATA OUTPUT** is the serial output signal for JTAG. TDO is driven on the falling edge of TCK during the SHIFT-IR and SHIFT-DR states of the Test Access Port. At other times, TDO floats.
TMS	**I** S(L)	**TEST MODE SELECT** is sampled at the rising edge of TCK to select the operation of the test logic for IEEE 1149.1 Boundary Scan testing. This signal has a weak internal pullup which is active during reset to ensure normal operation when the signal is not connected.

Table 5. Power Requirement, Processor Control and Test Signal Descriptions (Sheet 2 of 2)

NAME	TYPE	DESCRIPTION
TRST#	**I** A(L)	**TEST RESET** asynchronously resets the Test Access Port (TAP) controller function of IEEE 1149.1 Boundary Scan testing (JTAG). When using the Boundary Scan feature, connect a pulldown resistor (1.5 KΩ) between this signal and V_{SS}. When TAP is not used, this signal must be connected to V_{SS}; however, no resistor is required. The signal has a weak internal pullup which must be overcome during reset to ensure normal operation.
VCC	–	**POWER**. Connect to a 3.3 Volt V_{CC} board plane.
VCC5	–	**5 VOLT REFERENCE VOLTAGE.** Input is the reference voltage for the 5 V-tolerant I/O buffers. Connect this signal to +5 V for use with signals which exceed 3.3 V. When all inputs are from 3.3 V components, connect this signal to 3.3 V.
VSS	–	**GROUND.** Connect to a V_{SS} board plane.
N.C.	–	**NO CONNECT**. Do not make electrical connections to these balls.
VCCPLL3:1	**I**	**PLL POWER**. For external connection to a 3.3 V V_{CC} board plane. Power to PLLs requires external filtering.

Table 6. Interrupt Unit Signal Descriptions

NAME	TYPE	DESCRIPTION
NMI#	**I** A(L)	**NON-MASKABLE INTERRUPT** causes a non-maskable interrupt event to occur. NMI# is the highest priority interrupt source and is level-detect. When NMI# is unused, it is recommended that you connect it to V_{CC}.
S_INT[A:D]#/ XINT3:0#	**I** A(L)	**SECONDARY PCI BUS INTERRUPT**[1] requests an interrupt. S_INTx# assertion and deassertion is asynchronous to S_CLK. A device asserts S_INTx# when requesting attention from its device driver. When S_INTx# is asserted, it remains asserted until the device driver clears the pending request. S_INTx# Interrupts are level sensitive. **EXTERNAL INTERRUPT**. External devices use this signal to request an interrupt service. These signals operate in dedicated mode, where each signal is assigned a dedicated interrupt level. The S_INT[A:D]#/XINT3:0# signals can be directed as follows: **Sec. PCI** **Primary PCI** **80960 Core Processor** S_INTA# ⇒ P_INTA# or XINT0# S_INTB# ⇒ P_INTB# or XINT1# S_INTC# ⇒ P_INTC# or XINT2# S_INTD# ⇒ P_INTD# or XINT3#
XINT7:4#	**I** A(L)	**EXTERNAL INTERRUPT**. External devices use this signal to request an interrupt service. These signals operate in dedicated mode, where each signal is assigned a dedicated interrupt level.

NOTE:

1. PCI signal functions are summarized in this data sheet; refer to the *PCI Local Bus Specification* Revision 2.1 for a more complete definition.

Table 7. PCI Signal Descriptions (Sheet 1 of 3)

NAME	TYPE	DESCRIPTION[1]
P_AD31:0	**I/O** K(Q) R(Z)	**PRIMARY PCI ADDRESS/DATA** is the primary multiplexed PCI address and data bus.
P_C/BE3:0#	**I/O** K(Q) R(Z)	**PRIMARY PCI BUS COMMAND** and **BYTE ENABLE** signals are multiplexed on the same PCI signals. During an address phase, P_C/BE3:0# define the bus command. During a data phase, P_C/BE3:0# are used as byte enables.
P_DEVSEL#	**I/O** R(Z)	**PRIMARY PCI BUS DEVICE SELECT** is driven by a target agent that has successfully decoded the address. As an input, it indicates whether or not an agent has been selected.
P_FRAME#	**I/O** R(Z)	**PRIMARY PCI BUS CYCLE FRAME** is asserted to indicate the beginning and duration of an access on the Primary PCI bus.
P_GNT#	**I** R(Z)	**PRIMARY PCI BUS GRANT** indicates to the agent that access to the bus has been granted. This is a point-to-point signal.
P_IDSEL	**I** S(L)	**PRIMARY PCI BUS INITIALIZATION DEVICE SELECT** selects the 80960Rx during a Configuration Read or Write command on the primary PCI bus.
P_INT[A:D]#	**O** **OD** R(Z)	**PRIMARY PCI BUS INTERRUPT** requests an interrupt. The assertion and deassertion of P_INTx# is asynchronous to S_CLK. A device asserts its P_INTx# line when requesting attention from its device driver. Once the P_INTx# signal is asserted, it remains asserted until the device driver clears the pending request. P_INTx# Interrupts are level sensitive.
P_IRDY#	**I/O** R(Z)	**PRIMARY PCI BUS INITIATOR READY** indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction.
P_LOCK#	**I** S(L)	**PRIMARY PCI BUS LOCK** indicates an atomic operation that may require multiple transactions to complete.
P_PAR	**I/O** K(Q) R(Z)	**PRIMARY PCI BUS PARITY**. This signal ensures even parity across P_AD31:0 and P_C/BE3:0. All PCI devices must provide a parity signal.
P_PERR#	**I/O** R(Z)	**PRIMARY PCI BUS PARITY ERROR** is used for reporting data parity errors during all PCI transactions except a special cycle.
P_REQ#	**O** K(Q) R(Z)	**PRIMARY PCI BUS REQUEST** indicates to the arbiter that this agent desires use of the bus. This is a point to point signal.

NOTE:

1. PCI signal functions are summarized in this data sheet; refer to the *PCI Local Bus Specification* Revision 2.1 for a more complete definition.

Table 7. PCI Signal Descriptions (Sheet 2 of 3)

NAME	TYPE	DESCRIPTION[1]
P_RST#	**I** A(L)	**PRIMARY RESET** brings 80960Rx to a consistent state. When P_RST# is asserted: • PCI output signals are driven to a known consistent state. • PCI bus interface output signals are three-stated. • open drain signals such as P_SERR# are floated. • S_RST# asserts. P_RST# may be asynchronous to S_CLK when asserted or deasserted. Although asynchronous, deassertion must be guaranteed to be a clean, bounce-free edge.
P_SERR#	**I/O** **OD** R(Z)	**PRIMARY PCI BUS SYSTEM ERROR** reports address and data parity errors on the special cycle command, or any other system error where the result would be catastrophic.
P_STOP#	**I/O** R(Z)	**PRIMARY PCI BUS STOP** indicates that the current target is requesting the master to stop the current transaction on the primary PCI bus.
P_TRDY#	**I/O** R(Z)	**PRIMARY PCI BUS TARGET READY** indicates the target agent's (selected device's) ability to complete the current data phase of the transaction.
S_AD31:0	**I/O** R(0)	**SECONDARY PCI ADDRESS/DATA** is the secondary multiplexed PCI address and data bus. A bus transaction consists of an address phase followed by one or more data phases.
S_C/BE3:0#	**I/O** R(0)	**SECONDARY PCI BUS COMMAND and BYTE ENABLE** signals are multiplexed on the same PCI signals. During an address phase, S_C/BE3:0# define the bus command. During a data phase, S_C/BE3:0# are used as byte enables.
S_DEVSEL#	**I/O** R(Z)	**SECONDARY PCI BUS DEVICE SELECT** is driven by a target agent that has successfully decoded the address. As an input, it indicates whether or not an agent has been selected.
S_FRAME#	**I/O** R(Z)	**SECONDARY PCI BUS CYCLE FRAME** is asserted to indicate the beginning and duration of an access on the Secondary PCI bus.
S_GNT0#/ **S_REQ#**	**O** R(Z)	**SECONDARY PCI BUS GRANT0** is a grant signal sent to device 0 on the secondary PCI bus when the internal Secondary PCI Bus Arbiter is enabled. **SECONDARY PCI BUS REQUEST** is the request signal for the 80960Rx when the arbiter is disabled.
S_GNT5:1#	**O** R(Q)	**SECONDARY PCI BUS GRANT** are grant signals sent to devices 1-5 on the secondary PCI bus.
S_IDSEL	**I** S(L)	**SECONDARY PCI BUS INITIALIZATION DEVICE SELECT** selects the 80960Rx during a Configuration Read or Write command on the secondary PCI bus.
S_IRDY#	**I/O** R(Z)	**SECONDARY PCI BUS INITIATOR READY** indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction.

NOTE:

1. PCI signal functions are summarized in this data sheet; refer to the *PCI Local Bus Specification* Revision 2.1 for a more complete definition.

Table 7. PCI Signal Descriptions (Sheet 3 of 3)

NAME	TYPE	DESCRIPTION[1]
S_LOCK#	**I/O** R(Z)	**SECONDARY PCI BUS LOCK** indicates the need to perform an atomic operation on the secondary PCI bus.
S_PAR	**I/O** R(0)	**SECONDARY PCI BUS PARITY.** This signal ensures even parity across S_AD31:0 and S_C/BE3:0. All PCI devices must provide a parity signal.
S_PERR#	**I/O** R(Z)	**SECONDARY PCI BUS PARITY ERROR** is used for reporting data parity errors during all PCI transactions except a special cycle.
S_REQ0#/ S_GNT#	**I**	**SECONDARY PCI BUS REQUEST0** is a request signal from device 0 on the secondary PCI bus when the internal Secondary PCI Bus Arbiter is enabled. **SECONDARY PCI BUS GRANT** is the grant signal for the 80960Rx when the arbiter is disabled.
S_RST#	**O** R(Q)	**SECONDARY PCI BUS RESET** is an output based on P_RST#. It brings PCI-specific registers, sequencers, and signals to a consistent state. When P_RST# is asserted, it causes S_RST# to assert, and: • PCI output signals are driven to a known consistent state. • PCI bus interface output signals are three-stated. • open drain signals such as S_SERR# are floated. S_RST# may be asynchronous to S_CLK when asserted or deasserted.
S_SERR#	**I/O OD** R(Z)	**SECONDARY PCI BUS SYSTEM ERROR** reports address and data parity errors on the special cycle command, or any other system error where the result would be catastrophic.
S_STOP#	**I/O** R(Z)	**SECONDARY PCI BUS STOP** indicates that the current target is requesting the master to stop the current transaction on the secondary PCI bus.
S_TRDY#	**I/O** R(Z)	**SECONDARY PCI BUS TARGET READY** indicates the target agent's (selected device's) ability to complete the current data phase of the transaction.
S_REQ4:1#	**I** S(L)	**SECONDARY PCI BUS REQUEST 4:1** are request signals from devices 1-4 on the secondary PCI bus.
S_REQ5#/ S_ARB_EN	**I** S(L)	**SECONDARY PCI BUS REQUEST 5** is the request signal from device 5 on the secondary PCI bus. **SECONDARY PCI BUS ARBITER ENABLE** defines the power-up status of the internal secondary arbitration unit. A valid high at the deassertion of P_RST# enables the internal secondary arbiter. A valid low at the deassertion of P_RST# disables the internal secondary arbiter.

NOTE:

1. PCI signal functions are summarized in this data sheet; refer to the *PCI Local Bus Specification* Revision 2.1 for a more complete definition.

Table 8. Memory Controller Signal Descriptions (Sheet 1 of 2)

NAME	TYPE	DESCRIPTION
CAS7:0#	**O** R(1) H(Q) P(Q)	**COLUMN ADDRESS STROBE** signals are used for DRAM accesses and are asserted when the MA11:0 signals contain a valid column address. CAS7:0# signals are asserted during refresh. *Non-Interleaved Operation:* CAS0#,CAS4# = BE0# lane access CAS1#,CAS5# = BE1# lane access CAS2#,CAS6# = BE2# lane access CAS3#,CAS7# = BE3# lane access *Interleaved Operation:* CAS0# = BE0# Even leaf lane access CAS1# = BE1# Even leaf lane access CAS2# = BE2# Even leaf lane access CAS3# = BE3# Even leaf lane access CAS4# = BE0# Odd leaf lane access CAS5# = BE1# Odd leaf lane access CAS6# = BE2# Odd leaf lane access CAS7# = BE3# Odd leaf lane access
CE1:0#	**O** R(1) H(Q) P(Q)	**CHIP ENABLE** signals indicate an access to one of the two SRAM/ FLASH/ ROM memory banks. CE0# and CE1# are never asserted at the same time. These signals are valid during the entire memory operation. CE0# is asserted for accesses to memory bank 0. CE1# is asserted for accesses to memory bank 1.
DALE1:0	**O** R(0) H(Q) P(Q)	**DRAM ADDRESS LATCH ENABLE** signals support external address demultiplexing of the MA11:0 address lines for interleaved DRAM systems. Use these to directly interface to '373' type latches. These signals are only valid for accesses to interleaved memory systems. DALE0 is asserted during a valid even leaf address. DALE1 is asserted during a valid odd leaf address.
DP3:0	**I/O** R(X) H(Q) P(Q)	**DATA PARITY** carries the parity information for DRAM accesses. Each parity bit corresponds to a group of 8 data bus signals as follows: DP0 — AD7:0 DP2 — AD23:16 DP1 — AD15:8 DP3 — AD31:24 The memory controller generates parity information for local bus writes during data cycles. During read data cycles, the memory controller checks parity and provides notification of parity errors on the clock following the data cycle. Parity checking and polarity are user-programmable. Parity generation and checking are valid only for data lines that have their associated enable bits asserted.
DWE1:0#	**O** R(1) H(Q) P(Q)	**DRAM WRITE ENABLE** signals distinguish between read and write accesses to DRAM. DWE1:0# lines are asserted for writes and deasserted for reads. CAS7:0# determine valid bytes lanes during the access. These two outputs are functionally equivalent for all DRAM accesses; these provide increased drive capability for heavily loaded systems.
LEAF1:0#	**O** R(1) H(Q) P(Q)	**LEAF ENABLE** signals control the data output enables of the memory system during an interleaved DRAM read access. Use these to directly interface to either DRAM or transceiver output enable signals. LEAF0# is asserted during an even leaf access. LEAF1# is asserted during an odd leaf access.

Table 8. Memory Controller Signal Descriptions (Sheet 2 of 2)

NAME	TYPE	DESCRIPTION
MA11:0	**O** R(X) H(Q) P(Q)	**MULTIPLEXED ADDRESS** signals are multi-purpose depending on the device that is selected. For memory banks 0 and 1, these signals output address bits A13:2. These address bits are incremented for each data transfer of a burst access. For DRAM bank, these signals output the row/column multiplexed address bits 11:0. The relationship between the AD31:0 lines and the MA11:0 lines depends on the bank size, type and arrangement of the DRAM that is accessed.
MWE3:0#	**O** R(1) H(Q) P(Q)	**MEMORY WRITE ENABLE** signals for write accesses to SRAM/FLASH devices. The MWE's rising edge strobes valid data into these devices. MWE0# is asserted for writes to the BE0# lane MWE1# is asserted for writes to the BE1# lane MWE2# is asserted for writes to the BE2# lane MWE3# is asserted for writes to the BE3# lane
RAS3:0#	**O** R(1) H(Q) P(Q)	**ROW ADDRESS STROBE** signals are used for DRAM accesses and are asserted when the MA11:0 signals contain a valid row address. RAS3:0# always deasserts after the last data transfer in a DRAM access. *Non-Interleaved Operation:* RAS0# = Bank0 access RAS1# = Bank1 access RAS2# = Bank2 access RAS3# = Bank3 access *Interleaved Operation:* RAS0,2# = Even leaf RAS1,3# = Odd leaf

Table 9. DMA, APIC, I^2C Units Signal Descriptions (Sheet 1 of 2)

NAME	TYPE	DESCRIPTION
DACK#	**O** R(1) H(Q) P(Q)	**DMA DEMAND MODE ACKNOWLEDGE** The DMA Controller asserts this signal to indicate (1) it can receive new data from an external device or (2) it has data to send to an external device.
DREQ#	**I** S(L)	**DMA DEMAND MODE REQUEST** External devices use this signal to indicate (1) new data is ready for transfer to the DMA controller or (2) buffers are available to receive data from the DMA controller.
PICCLK	**I**	**APIC BUS CLOCK** provides synchronous operation of the APIC bus.
PICD1:0	**I/O OD** R(Z) H(Q) P(Q)	**APIC DATA** lines comprise the data portion of the APIC 3-wire bus.

Table 9. DMA, APIC, I²C Units Signal Descriptions (Sheet 2 of 2)

NAME	TYPE	DESCRIPTION
SCL	**I/O** **OD** R(Z) H(Q) P(Q)	**I²C CLOCK** provides synchronous I²C bus operation.
SDA	**I/O** **OD** R(Z) H(Q) P(Q)	**I²C DATA** used for data transfer and arbitration on the I²C bus.
WAIT#	**O** R(1) H(Q) P(Q)	**WAIT** is an output that allows the DMA controller to insert wait states during DMA accesses to an external memory system.

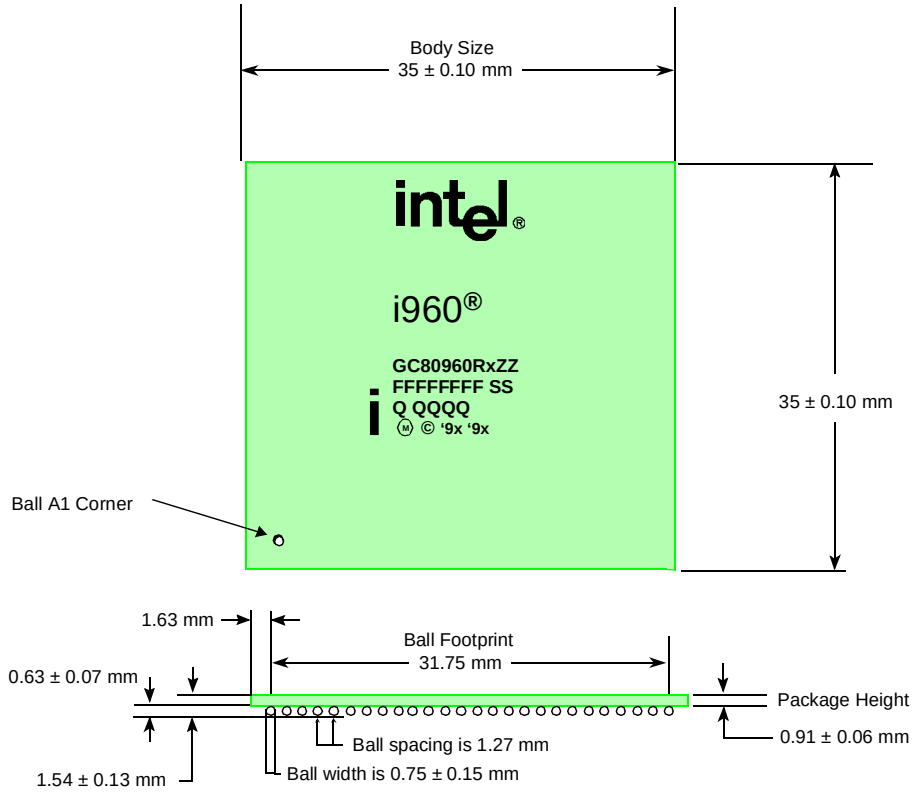
Table 10. Clock Signal

NAME	TYPE	DESCRIPTION
S_CLK	**I**	**SYNCHRONOUS PCI BUS CLOCK** Provides the processor's fundamental time base. All input/output timings are relative to S_CLK.

Table 11. ICE Signal Descriptions

NAME	TYPE	DESCRIPTION
ICEADS#	**O**	**ICE ADDRESS/DATA STATUS** indicates a valid address and the start of a new bus access. ICEADS# is active for accesses to external microcode.
ICEBRK#	**I**	**ICE BREAK** forces the processor to transition from emulation to interrogation mode.
ICEBUS7:0	**I/O**	**ICE BUS** is a bidirectional 8-bit bus linking the processor and the emulator. Used in various modes.
ICECLK	**O**	**ICE CLOCK** output signal to which all ICE bus signals are synchronized.
ICELOCK#	**I**	**ICE LOCK** is sampled during 80960 core reset to protect ICE configuration.
ICEMSG#	**I**	**ICE MESSAGE** signal used to acknowledge data from the processor to the emulator. Used only during interrogation mode.
ICESEL#	**I**	**ICESEL** enables or disables the ICE unit.
ICEVLD#	**O**	**ICE VALID** indicates the processor is driving the ICEBUS with valid data.
MSGFRM#	**O**	**ICE MESSAGE FRAME** indicates that trace messages are being issued to the ICEBUS. Used in emulation mode only.

3.1.2 352-Lead HL-PBGA Package



NOTES:

1. All dimensions and tolerances conform to ANSI Y14.5M 1982.
2. All dimensions are in millimeters.
3. Tin/Lead mix: 63%/37%.
4. Pad plating method: Electrolytic.
5. Encapsulant size: 22.38 x 22.38 mm (max).

Figure 3. 352L HL-PBGA Package Diagram (Top and Side View)

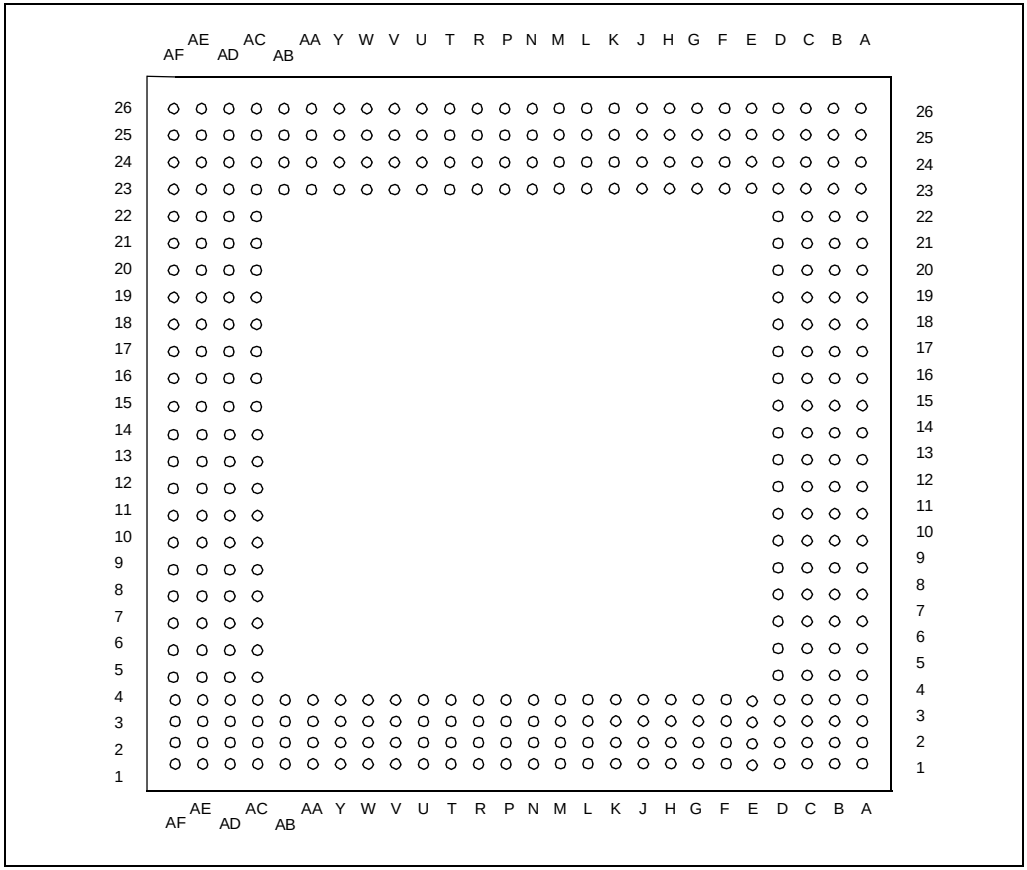


Figure 4. 352L HL-PBGA Package Diagram (Bottom View)

Table 12. 352-Lead HL-PBGA Package — Signal Name Order (Sheet 1 of 4)

Signal	Ball #	Signal	Ball #	Signal	Ball #
AD0	**A18**	CAS0#	**F1**	ICESEL#	**AC2**
AD1	**B18**	CAS1#	**F2**	ICEVLD#	**AB1**
AD2	**C17**	CAS2#	**G3**	LEAF0	**L2**
AD3	**A17**	CAS3#	**G1**	LEAF1	**M3**
AD4	**B17**	CAS4#	**G2**	LOCK#/ONCE#	**AD4**
AD5	**C16**	CAS5#	**H3**	LRDYRCV#	**C19**
AD6	**A16**	CAS6#	**H1**	LRST#	**AD6**
AD7	**B16**	CAS7#	**H2**	MA0	**C7**
AD8	**C15**	CE0#	**L3**	MA1	**A7**
AD9	**A15**	CE1#	**L1**	MA2	**B7**
AD10	**B15**	D/C#/RST_MODE#	**AF4**	MA3	**C6**
AD11	**C14**	DACK#	**AD3**	MA4	**B6**
AD12	**A14**	DALE0	**M1**	MA5	**C5**
AD13	**B14**	DALE1	**M2**	MA6	**A5**
AD14	**C13**	DEN#	**A23**	MA7	**B5**
AD15	**A13**	DP0	**C2**	MA8	**C4**
AD16	**B13**	DP1	**D3**	MA9	**B4**
AD17	**C12**	DP2	**D1**	MA10	**C3**
AD18	**A12**	DP3	**D2**	MA11	**B3**
AD19	**B12**	DREQ#	**AD2**	MSGFRM#	**AC3**
AD20	**C11**	DT/R#	**B23**	MWE0#	**J3**
AD21	**A11**	DWE0#	**K1**	MWE1#	**J1**
AD22	**B11**	DWE1#	**K2**	MWE2#	**J2**
AD23	**C10**	FAIL#	**AD5**	MWE3#	**K3**
AD24	**A10**	HOLD	**V1**	NC	**A20**
AD25	**B10**	HOLDA	**V3**	NC	**AE4**
AD26	**C9**	ICEADS#	**AC1**	NC	**B20**
AD27	**A9**	ICEBRK#	**AA1**	NC	**C18**
AD28	**B9**	ICEBUS0	**V2**	NMI#	**T3**
AD29	**C8**	ICEBUS1	**W3**	P_AD0	**AD24**
AD30	**A8**	ICEBUS2	**W1**	P_AD1	**AE23**
AD31	**B8**	ICEBUS3	**W2**	P_AD2	**AF23**
ADS#	**B21**	ICEBUS4	**Y3**	P_AD3	**AD23**
ALE	**C20**	ICEBUS5	**Y1**	P_AD4	**AE22**
BE0#	**A22**	ICEBUS6	**Y2**	P_AD5	**AF22**
BE1#	**B22**	ICEBUS7	**AA3**	P_AD6	**AD22**
BE2#	**C21**	ICECLK	**AB2**	P_AD7	**AE21**
BE3#	**A21**	ICELOCK#	**AB3**	P_AD8	**AD21**
BLAST#	**C23**	ICEMSG#	**AA2**	P_AD9	**AE20**

Table 12. 352-Lead HL-PBGA Package — Signal Name Order (Sheet 2 of 4)

Signal	Ball #	Signal	Ball #	Signal	Ball #
P_AD10	**AF20**	P_RST#	**AE7**	S_AD27	**K24**
P_AD11	**AD20**	P_SERR#	**AE17**	S_AD28	**K26**
P_AD12	**AE19**	P_STOP#	**AE16**	S_AD29	**K25**
P_AD13	**AF19**	P_TRDY#	**AD16**	S_AD30	**J24**
P_AD14	**AD19**	PICCLK	**U3**	S_AD31	**J26**
P_AD15	**AE18**	PICD0	**T1**	S_C/BE0#	**AA24**
P_AD16	**AE14**	PICD1	**T2**	S_C/BE1#	**V24**
P_AD17	**AF14**	RAS0#	**E3**	S_C/BE2#	**R26**
P_AD18	**AD14**	RAS1#	**E1**	S_C/BE3#	**M25**
P_AD19	**AE13**	RAS2#	**E2**	S_CLK	**F25**
P_AD20	**AF13**	RAS3#	**F3**	S_DEVSEL#	**T24**
P_AD21	**AD13**	RDYRCV#	**B19**	S_FRAME#	**R24**
P_AD22	**AE12**	S_AD0	**AE24**	S_GNT0#/S_REQ#	**H26**
P_AD23	**AF12**	S_AD1	**AD25**	S_GNT1#	**G24**
P_AD24	**AF11**	S_AD2	**AC24**	S_GNT2#	**G25**
P_AD25	**AD11**	S_AD3	**AC26**	S_GNT3#	**F26**
P_AD26	**AE10**	S_AD4	**AC25**	S_GNT4#	**E26**
P_AD27	**AF10**	S_AD5	**AB24**	S_GNT5#	**D24**
P_AD28	**AD10**	S_AD6	**AB26**	S_IDSEL	**M26**
P_AD29	**AE9**	S_AD7	**AB25**	S_INTA#/XINT0#	**N1**
P_AD30	**AF9**	S_AD8	**AA26**	S_INTB#/XINT1#	**N2**
P_AD31	**AD9**	S_AD9	**AA25**	S_INTC#/XINT2#	**P3**
P_C/BE0#	**AF21**	S_AD10	**Y24**	S_INTD#/XINT3#	**P1**
P_C/BE1#	**AF18**	S_AD11	**Y26**	S_IRDY#	**T25**
P_C/BE2#	**AD15**	S_AD12	**Y25**	S_LOCK#	**U26**
P_C/BE3#	**AE11**	S_AD13	**W24**	S_PAR	**V26**
P_DEVSEL#	**AF16**	S_AD14	**W26**	S_PERR#	**U24**
P_FRAME#	**AF15**	S_AD15	**W25**	S_REQ0#/S_GNT#	**H24**
P_GNT#	**AF8**	S_AD16	**R25**	S_REQ1#	**H25**
P_IDSEL	**AD12**	S_AD17	**P24**	S_REQ2#	**G26**
P_INTA#	**AF6**	S_AD18	**P26**	S_REQ3#	**F24**
P_INTB#	**AE6**	S_AD19	**P25**	S_REQ4#	**E24**
P_INTC#	**AD7**	S_AD20	**N24**	S_REQ5#/S_ARB_EN	**E25**
P_INTD#	**AF7**	S_AD21	**N26**	S_RST#	**J25**
P_IRDY#	**AE15**	S_AD22	**N25**	S_SERR#	**V25**
P_LOCK#	**AD17**	S_AD23	**M24**	S_STOP#	**U25**
P_PAR	**AD18**	S_AD24	**L24**	S_TRDY#	**T26**
P_PERR#	**AF17**	S_AD25	**L26**	SCL	**U1**
P_REQ#	**AE8**	S_AD26	**L25**	SDA	**U2**

Table 12. 352-Lead HL-PBGA Package — Signal Name Order (Sheet 3 of 4)

Signal	Ball #	Signal	Ball #	Signal	Ball #
STEST	AE3	V_{CC}	B25	V_{SS}	AC7
TCK	B24	V_{CC}	B26	V_{SS}	AC9
TDI	D26	V_{CC}	C1	V_{SS}	AC11
TDO	D25	V_{CC}	C26	V_{SS}	AC13
TMS	C24	V_{CC}	D5	V_{SS}	AC15
TRST#	C25	V_{CC}	D7	V_{SS}	AC17
V_{CC}	A1	V_{CC}	D9	V_{SS}	AC19
V_{CC}	A2	V_{CC}	D11	V_{SS}	AC21
V_{CC}	A24	V_{CC}	D13	V_{SS}	AC23
V_{CC}	A25	V_{CC}	D15	V_{SS}	D4
V_{CC}	A26	V_{CC}	D17	V_{SS}	D6
V_{CC}	AA23	V_{CC}	D19	V_{SS}	D8
V_{CC}	AB4	V_{CC}	D21	V_{SS}	D10
V_{CC}	AC6	V_{CC}	E23	V_{SS}	D12
V_{CC}	AC8	V_{CC}	F4	V_{SS}	D14
V_{CC}	AC10	V_{CC}	G23	V_{SS}	D16
V_{CC}	AC12	V_{CC}	H4	V_{SS}	D18
V_{CC}	AC14	V_{CC}	J23	V_{SS}	D20
V_{CC}	AC16	V_{CC}	K4	V_{SS}	D22
V_{CC}	AC18	V_{CC}	L23	V_{SS}	D23
V_{CC}	AC20	V_{CC}	M4	V_{SS}	E4
V_{CC}	AC22	V_{CC}	N23	V_{SS}	F23
V_{CC}	AD1	V_{CC}	P4	V_{SS}	G4
V_{CC}/V_{SS} (1)	AD8	V_{CC}	R23	V_{SS}	H23
V_{CC}	AD26	V_{CC}	T4	V_{SS}	J4
V_{CC}	AE1	V_{CC}	U23	V_{SS}	K23
V_{CC}	AE2	V_{CC}	V4	V_{SS}	L4
V_{CC}	AE25	V_{CC}	W23	V_{SS}	M23
V_{CC}	AE26	V_{CC}	Y4	V_{SS}	N4
V_{CC}	AF1	V_{CC5}	A3	V_{SS}	P23
V_{CC}	AF2	VCCPLL1	A19	V_{SS}	R4
V_{CC}	AF3	VCCPLL2	A6	V_{SS}	T23
V_{CC}	AF24	VCCPLL3	A4	V_{SS}	U4
V_{CC}	AF25	V_{SS}	AA4	V_{SS}	V23
V_{CC}	AF26	V_{SS}	AB23	V_{SS}	W4
V_{CC}	B1	V_{SS}	AC4	V_{SS}	Y23
V_{CC}	B2	V_{SS}	AC5	W/R#	C22

NOTES:

1. Ball AD8 must be tied to either V_{CC} or V_{SS}.

Table 12. 352-Lead HL-PBGA Package — Signal Name Order (Sheet 4 of 4)

Signal	Ball #	Signal	Ball #	Signal	Ball #
WAIT#	**N3**	XINT4#	**P2**	XINT7#	**R2**
WIDTH/HLTD0	**AF5**	XINT5#	**R3**		
WIDTH/HLTD1/RETRY	**AE5**	XINT6#	**R1**		

Table 13. 352-Lead HL-PBGA Pinout — Ballpad Number Order (Sheet 1 of 4)

Ball #	Signal	Ball #	Signal	Ball #	Signal
A1	V_{CC}	**B10**	AD25	**C19**	LRDYRCV#
A2	V_{CC}	**B11**	AD22	**C20**	ALE
A3	V_{CC5}	**B12**	AD19	**C21**	BE2#
A4	VCCPLL3	**B13**	AD16	**C22**	W/R#
A5	MA6	**B14**	AD13	**C23**	BLAST#
A6	VCCPLL2	**B15**	AD10	**C24**	TMS
A7	MA1	**B16**	AD7	**C25**	TRST#
A8	AD30	**B17**	AD4	**C26**	V_{CC}
A9	AD27	**B18**	AD1	**D1**	DP2
A10	AD24	**B19**	RDYRCV#	**D2**	DP3
A11	AD21	**B20**	NC	**D3**	DP1
A12	AD18	**B21**	ADS#	**D4**	V_{SS}
A13	AD15	**B22**	BE1#	**D5**	V_{CC}
A14	AD12	**B23**	DT/R#	**D6**	V_{SS}
A15	AD9	**B24**	TCK	**D7**	V_{CC}
A16	AD6	**B25**	V_{CC}	**D8**	V_{SS}
A17	AD3	**B26**	V_{CC}	**D9**	V_{CC}
A18	AD0	**C1**	V_{CC}	**D10**	V_{SS}
A19	VCCPLL1	**C2**	DP0	**D11**	V_{CC}
A20	NC	**C3**	MA10	**D12**	V_{SS}
A21	BE3#	**C4**	MA8	**D13**	V_{CC}
A22	BE0#	**C5**	MA5	**D14**	V_{SS}
A23	DEN#	**C6**	MA3	**D15**	V_{CC}
A24	V_{CC}	**C7**	MA0	**D16**	V_{SS}
A25	V_{CC}	**C8**	AD29	**D17**	V_{CC}
A26	V_{CC}	**C9**	AD26	**D18**	V_{SS}
B1	V_{CC}	**C10**	AD23	**D19**	V_{CC}
B2	V_{CC}	**C11**	AD20	**D20**	V_{SS}
B3	MA11	**C12**	AD17	**D21**	V_{CC}
B4	MA9	**C13**	AD14	**D22**	V_{SS}
B5	MA7	**C14**	AD11	**D23**	V_{SS}
B6	MA4	**C15**	AD8	**D24**	S_GNT5#
B7	MA2	**C16**	AD5	**D25**	TDO
B8	AD31	**C17**	AD2	**D26**	TDI
B9	AD28	**C18**	NC	**E1**	RAS1#

Table 13. 352-Lead HL-PBGA Pinout — Ballpad Number Order (Sheet 2 of 4)

Ball #	Signal	Ball #	Signal	Ball #	Signal
E2	RAS2#	J23	V_{CC}	N26	S_AD21
E3	RAS0#	J24	S_AD30	P1	S_INTD#/XINT3#
E4	V_{SS}	J25	S_RST#	P2	XINT4#
E23	V_{CC}	J26	S_AD31	P3	S_INTC#/XINT2#
E24	S_REQ4#	K1	DWE0#	P4	V_{CC}
E25	S_REQ5#/S_ARB_EN	K2	DWE1#	P23	V_{SS}
E26	S_GNT4#	K3	MWE3#	P24	S_AD17
F1	CAS0#	K4	V_{CC}	P25	S_AD19
F2	CAS1#	K23	V_{SS}	P26	S_AD18
F3	RAS3#	K24	S_AD27	R1	XINT6#
F4	V_{CC}	K25	S_AD29	R2	XINT7#
F23	V_{SS}	K26	S_AD28	R3	XINT5#
F24	S_REQ3#	L1	CE1#	R4	V_{SS}
F25	S_CLK	L2	LEAF0#	R23	V_{CC}
F26	S_GNT3#	L3	CE0#	R24	S_FRAME#
G1	CAS3#	L4	V_{SS}	R25	S_AD16
G2	CAS4#	L23	V_{CC}	R26	S_C/BE2#
G3	CAS2#	L24	S_AD24	T1	PICD0
G4	V_{SS}	L25	S_AD26	T2	PICD1
G23	V_{CC}	L26	S_AD25	T3	NMI#
G24	S_GNT1#	M1	DALE0	T4	V_{CC}
G25	S_GNT2#	M2	DALE1	T23	V_{SS}
G26	S_REQ2#	M3	LEAF1#	T24	S_DEVSEL#
H1	CAS6#	M4	V_{CC}	T25	S_IRDY#
H2	CAS7#	M23	V_{SS}	T26	S_TRDY#
H3	CAS5#	M24	S_AD23	U1	SCL
H4	V_{CC}	M25	S_C/BE3#	U2	SDA
H23	V_{SS}	M26	S_IDSEL	U3	PICCLK
H24	S_REQ0#/S_GNT#	N1	S_INTA#/XINT0#	U4	V_{SS}
H25	S_REQ1#	N2	S_INTB#/XINT1#	U23	V_{CC}
H26	S_GNT0#/S_REQ#	N3	WAIT#	U24	S_PERR#
J1	MWE1#	N4	V_{SS}	U25	S_STOP#
J2	MWE2#	N23	V_{CC}	U26	S_LOCK#
J3	MWE0#	N24	S_AD20	V1	HOLD
J4	V_{SS}	N25	S_AD22	V2	ICEBUS0

Table 13. 352-Lead HL-PBGA Pinout — Ballpad Number Order (Sheet 3 of 4)

Ball #	Signal	Ball #	Signal	Ball #	Signal
V3	HOLDA	AB4	V_{CC}	AD3	DACK#
V4	V_{CC}	AB23	V_{SS}	AD4	LOCK#/ONCE#
V23	V_{SS}	AB24	S_AD5	AD5	FAIL#
V24	S_C/BE1#	AB25	S_AD7	AD6	LRST#
V25	S_SERR#	AB26	S_AD6	AD7	P_INTC#
V26	S_PAR	AC1	ICEADS#	AD8	V_{CC}/V_{SS} (1)
W1	ICEBUS2	AC2	ICESEL#	AD9	P_AD31
W2	ICEBUS3	AC3	MSGFRM#	AD10	P_AD28
W3	ICEBUS1	AC4	V_{SS}	AD11	P_AD25
W4	V_{SS}	AC5	V_{SS}	AD12	P_IDSEL
W23	V_{CC}	AC6	V_{CC}	AD13	P_AD21
W24	S_AD13	AC7	V_{SS}	AD14	P_AD18
W25	S_AD15	AC8	V_{CC}	AD15	P_C/BE2#
W26	S_AD14	AC9	V_{SS}	AD16	P_TRDY#
Y1	ICEBUS5	AC10	V_{CC}	AD17	P_LOCK#
Y2	ICEBUS6	AC11	V_{SS}	AD18	P_PAR
Y3	ICEBUS4	AC12	V_{CC}	AD19	P_AD14
Y4	V_{CC}	AC13	V_{SS}	AD20	P_AD11
Y23	V_{SS}	AC14	V_{CC}	AD21	P_AD8
Y24	S_AD10	AC15	V_{SS}	AD22	P_AD6
Y25	S_AD12	AC16	V_{CC}	AD23	P_AD3
Y26	S_AD11	AC17	V_{SS}	AD24	P_AD0
AA1	ICEBRK#	AC18	V_{CC}	AD25	S_AD1
AA2	ICEMSG#	AC19	V_{SS}	AD26	V_{CC}
AA3	ICEBUS7	AC20	V_{CC}	AE1	V_{CC}
AA4	V_{SS}	AC21	V_{SS}	AE2	V_{CC}
AA23	V_{CC}	AC22	V_{CC}	AE3	STEST
AA24	S_C/BE0#	AC23	V_{SS}	AE4	NC
AA25	S_AD9	AC24	S_AD2	AE5	WIDTH/HLTD1/RETRY
AA26	S_AD8	AC25	S_AD4	AE6	P_INTB#
AB1	ICEVLD#	AC26	S_AD3	AE7	P_RST#
AB2	ICECLK	AD1	V_{CC}	AE8	P_REQ#
AB3	ICELOCK#	AD2	DREQ#	AE9	P_AD29

NOTES:

1. Ball AD8 must be tied to either V_{CC} or V_{SS}.

Table 13. 352-Lead HL-PBGA Pinout — Ballpad Number Order (Sheet 4 of 4)

Ball #	Signal	Ball #	Signal	Ball #	Signal
AE10	P_AD26	**AE25**	V_{CC}	**AF14**	P_AD17
AE11	P_C/BE3#	**AE26**	V_{CC}	**AF15**	P_FRAME#
AE12	P_AD22	**AF1**	V_{CC}	**AF16**	P_DEVSEL#
AE13	P_AD19	**AF2**	V_{CC}	**AF17**	P_PERR#
AE14	P_AD16	**AF3**	V_{CC}	**AF18**	P_C/BE1#
AE15	P_IRDY#	**AF4**	D/C#/RST_MODE#	**AF19**	P_AD13
AE16	P_STOP#	**AF5**	WIDTH/HLTD0	**AF20**	P_AD10
AE17	P_SERR#	**AF6**	P_INTA#	**AF21**	P_C/BE0#
AE18	P_AD15	**AF7**	P_INTD#	**AF22**	P_AD5
AE19	P_AD12	**AF8**	P_GNT#	**AF23**	P_AD2
AE20	P_AD9	**AF9**	P_AD30	**AF24**	V_{CC}
AE21	P_AD7	**AF10**	P_AD27	**AF25**	V_{CC}
AE22	P_AD4	**AF11**	P_AD24	**AF26**	V_{CC}
AE23	P_AD1	**AF12**	P_AD23		
AE24	S_AD0	**AF13**	P_AD20		

3.2 Package Thermal Specifications

The device is specified for operation when T_C (case temperature) is within the range of 0° C to 95° C. Case temperature may be measured in any environment to determine whether the processor is within specified operating range. Measure the case temperature at the center of the top surface, opposite the ballpad.

3.2.1 Thermal Specifications

This section defines the terms used for thermal analysis.

3.2.1.1 Ambient Temperature

Ambient temperature, T_A, is the temperature of the ambient air surrounding the package. In a system environment, ambient temperature is the temperature of the air upstream from the package.

3.2.1.2 Case Temperature

To ensure functionality and reliability, the device is specified for proper operation when the case temperature, T_C, is within the specified range in Table 16, Operating Conditions (pg. 34).

When measuring case temperature, attention to detail is required to ensure accuracy. If a thermocouple is used, calibrate it before taking measurements. Errors may result when the measured surface temperature is affected by the surrounding ambient air temperature. Such errors may be due to a poor thermal contact between thermocouple junction and the surface, heat loss by radiation, or conduction through thermocouple leads.

To minimize measurement errors:

- Use a 35 gauge K-type thermocouple or equivalent.
- Attach the thermocouple bead or junction to the package top surface at a location corresponding to the center of the die (Figure 5). The center of the die gives a more accurate measurement and less variation as the boundary condition changes.
- Attach the thermocouple bead or junction at a 90° angle by an adhesive bond (such as thermal epoxy or heat-tolerant tape) to the package top surface as shown in Figure 5. When a heat sink is attached, drill a hole through the heat sink to allow contact with the package above the center of the die. The hole diameter should be no larger than 3.8 mm as shown in Figure 6.

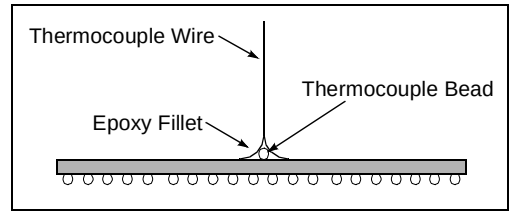


Figure 5. Thermocouple Attachment - No Heat Sink

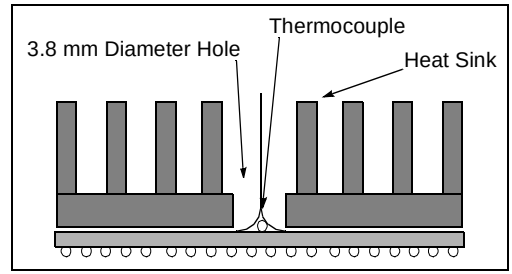


Figure 6. Thermocouple Attachment - With Heat Sink

3.2.1.3 Thermal Resistance

The thermal resistance value for the case-to-ambient, θ_{CA}, is used as a measure of the cooling solution's thermal performance.

3.2.2 Thermal Analysis

This thermal analysis is based on the following assumptions:

- Power dissipation is a constant 5 W.
- Maximum case temperature is 95° C.

Table 14 lists the case-to-ambient thermal resistances of the 80960RP for different air flow rates with and without a heat sink.

To calculate T_A, the maximum ambient temperature to conform to a particular case temperature:

$$T_A = T_C - P (\theta_{CA})$$

Compute P by multiplying I_{CC} and V_{CC}. Valuesfor θ_{JC} and θ_{CA} are given in Table 14.

Junction temperature (T_J) is commonly used in reliability calculations. T_J can be calculated from θ_{JC} (thermal resistance from junction to case) using the following equation:

$$T_J = T_C + P (\theta_{JC})$$

Similarly, when T_A is known, the corresponding case temperature (T_C) can be calculated as follows:

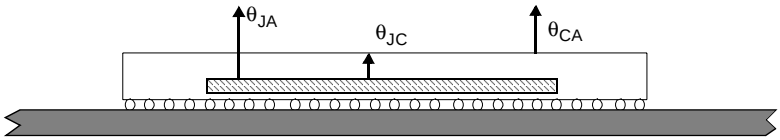
$$T_C = T_A + P (\theta_{CA})$$

The θ_{JA} (Junction to Ambient) for this package is currently estimated at 9.74° C/Watt with no airflow.

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

Table 14. 352-Lead HL-PBGA Package Thermal Characteristics

Thermal Resistance — °C/Watt								
Parameter	**Airflow — ft./min (m/sec)**							
	0 (0)	**50 (0.25)**	**100 (0.50)**	**200 (1.01)**	**300 (1.52)**	**400 (2.03)**	**600 (3.04)**	**800 (4.06)**
θ_{JC} (Junction-to-Case)	0.60	0.60	0.60	0.60	0.60	0.60	0.60	0.60
θ_{CA} (Case-to-Ambient) Without Heatsink	9.14	7.64	6.58	6.11	5.79	5.61	5.49	5.47
θ_{CA} (Case-to-Ambient) With Heatsink[2]	7.31	6.00	5.21	4.80	4.52	4.37	4.26	4.23



NOTES:

1. This table applies to a HL-PBGA device soldered directly onto a board.
2. See Table 15 for heatsink information.

3.3 Sources for Heatsinks and Accessories

The following is a list of suggested sources for heatsinks and accessories. This is neither an endorsement nor a warranty of the performance of any of the listed products and/or companies.

Table 15. Heatsink Information

Manufacturer	Part No.	Heatsink Dimensions (mm)	Product Description
Thermalloy, Inc. 2021 West Valley View Lane Dallas, TX 75234-8993 Tel: (214) 243-4321 FAX: (214) 241-4656	Heatsink: 2338B BGA Clip: 20812-2	32 X 34 X 12.6	Thermalloy Heatsink; use with BGA Clip and Parker Chromerics Thermflow tape
Parker Chromerics 77 Dragon Court Woburn, MA 01888 Tel: (617) 935-4850 FAX: (617) 933-4318	T705	NA	Thermflow tape; use with Thermalloy BGA Clip
AAVID Thermal Technologies, Inc. One Kool Path P.O. Box 400 Laconia, N.H. 13247-0400 Tel: (603) 528-3400 FAX: (603) 527-2129	Heatsink: 364424B00032	40.5 X 40 X 11	AAVID Heatsink; use with pre-applied thermal adhesive tape (Ther-A-Grip)

4.0 ELECTRICAL SPECIFICATIONS

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Contact your local Intel representative before finalizing a design.

4.1 Absolute Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	–55° C to + 125° C
Case Temperature Under Bias	0° C to + 95° C
Supply Voltage wrt. V_{SS}	–0.5 V to + 4.6 V
Supply Voltage wrt. V_{SS} on V_{CC5}	–0.5 V to + 6.5 V
Voltage on Any Ball wrt. V_{SS}	–0.5 V to V_{CC} + 0.5 V

WARNING: *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Table 16. Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
V_{CC}	Supply Voltage	3.0	3.6	V	
V_{CC5}	Input Protection Bias	3.0	5.25	V	
F_{S_CLK}	Input Clock Frequency	16	33.33	MHz	
T_C	Case Temperature Under Bias GC80960Rx (352 HL-PBGA)	0	95	°C	

4.2 V_{CC5} Pin Requirements (V_{DIFF})

In mixed voltage systems that drive 80960Rx processor inputs in excess of 3.3 V, the V_{CC5} pin must be connected to the system's 5 V supply. To limit current flow into the V_{CC5} pin, there is a limit to the voltage differential between the V_{CC5} pin and the other V_{CC} pins. The voltage differential between the 80960Rx V_{CC5} pin and its 3.3 V V_{CC} pins should never exceed 2.25 V. This limit applies to power-up, power-down, and steady-state operation. Table 17 outlines this requirement.

Meeting this requirement ensures proper operation and guarantees that the current draw into the V_{CC5} pin does not exceed the I_{CC5} specification.

If the voltage difference requirements cannot be met due to system design limitations, an alternate solution may be employed. As shown in Figure 7, a minimum of 100 Ω series resistor may be used to limit the current into the V_{CC5} pin. This resistor ensures that current drawn by the V_{CC5} pin does not exceed the maximum rating for this pin.

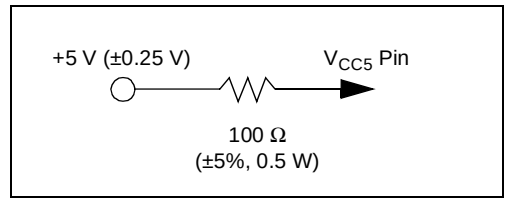


Figure 7. VCC5 Current-Limiting Resistor

This resistor is not necessary in systems that can guarantee the V_{DIFF} specification.

In 3.3 V-only systems and systems that drive 80960Rx pins from 3.3 V logic, connect the V_{CC5} pin directly to the 3.3 V V_{CC} plane.

Table 17. V_{DIFF} Specification for Dual Power Supply Requirements (3.3 V, 5 V)

Symbol	Parameter	Min	Max	Units	Notes
V_{DIFF}	V_{CC5}-V_{CC} Difference		2.25	V	V_{CC5} input should not exceed V_{CC} by more than 2.25 V during power-up and power-down, or during steady-state operation.

4.3 Targeted DC Specifications

Table 18. DC Characteristics

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage	-0.5	0.8	V	(1)
V_{IH1}	Input High Voltage for all signals except SCLK	2.0	V_{CC} + 0.5	V	(1)
V_{IH2}	Input High Voltage for SCLK	2.1	V_{CC} + 0.5	V	(1)
V_{OL1}	Output Low Voltage Processor signals		0.45	V	I_{OL} = 6 mA (3)
V_{OH1}	Output High Voltage Processor signals	2.4 V_{CC} - 0.5		V	I_{OH} = -2 mA (3) I_{OH} = -200 µA (3)
V_{OL2}	Output Low Voltage PCI signals		0.55	V	I_{OL} = 6 mA (1)
V_{OH2}	Output High Voltage PCI signals	2.4		V	I_{OH} = -2 mA (1)
V_{OL3}	Output Low Voltage Memory Controller Normal drive		0.45	V	I_{OL} = 6 mA (4)
V_{OH3}	Output High Voltage Memory Controller Normal drive	2.4		V	I_{OH} = -2 mA (4)
V_{OL4}	Output Low Voltage Memory Controller High Drive		0.45	V	I_{OL} = 7 mA
V_{OH4}	Output High Voltage Memory Controller High Drive	2.4		V	I_{OH} = -2 mA
V_{OL5}	Output Low Voltage APIC Data Lines		0.45	V	I_{OL} = 10 mA
C_{IN}	Input Capacitance - HL-PBGA		10	pF	F_{S_CLK} = T_F Min (1, 2)
C_{OUT}	I/O or Output Capacitance - HL-PBGA		10	pF	F_{S_CLK} = T_F Min (1, 2)
C_{CLK}	S_CLK Capacitance - HL-PBGA	5	12	pF	F_{S_CLK} = T_F Min (1, 2)
C_{IDSEL}	IDSEL Ball Capacitance		8	pF	(1)
L_{PIN}	Ball Inductance		20	nH	(1)

NOTES:

1. As required by the *PCI Local Bus Specification* Revision 2.1.
2. Not tested.
3. Processor signals include AD31:0, ALE, ADS#, BE3:0#, WIDTH/HLTD0, WIDTH/HLTD1/RETRY, D/C#/RST_MODE#, W/R#, DT/R#, DEN#, BLAST#, LRDYRCV#, LOCK#/ONCE#, HOLD, FAIL#, TDO, DACK#, WAIT#, SDA, SCL.
4. Memory Controller signals include MA11:0, DP3:0, RAS3:0#, CAS7:0#, MWE3:0#, DWE1:0#, DALE1:0, CE1:0#, LEAF1:0#.
5. Memory Controller signals capable of high drive are MA11:0, CAS7:0#, RAS3:0#, DWE1:0#.

Table 19. I_{CC} Characteristics

Symbol	Parameter	Typ	Max	Units	Notes
I_{LI1}	Input Leakage Current for each signal except PCI Bus Signals, LOCK#/ONCE#, WIDTH/HLTD0, WIDTH/HLTD1/RETRY, BLAST#, D/C#/RST_MODE#, DEN#,TMS, TRST#, TDI		± 80	µA	$0 \le V_{IN} \le V_{CC}$
I_{LI2}	Input Leakage Current for LOCK#/ONCE#, WIDTH/HLTD0, WIDTH/HLTD1/RETRY, BLAST#, D/C#/RST_MODE#, DEN#, TMS, TRST#, TDI	-140	-250	µA	V_{IN} = 0.45 V (1)
I_{LI3}	Input Leakage Current for PCI Bus Signals		± 5	µA	$0 \le V_{IN} \le V_{CC}$
I_{LO}	Output Leakage Current		± 5	µA	$0.4 \le V_{OUT} \le V_{CC}$
I_{CC} Active (Power Supply)	Power Supply Current 80960RP 33/3.3 80960RD 66/3.3		 1.00 1.30	A	(1,2)
I_{CC} Active (Thermal)	Thermal Current 80960RP 33/3.3 80960RD 66/3.3	 0.75 0.95		A	(1,3)
I_{CC} Active (Power Modes)	Reset Mode 80960RP 33/3.3 80960RD 66/3.3 ONCE Mode 80960RP 33/3.3 80960RD 66/3.3		 0.65 0.80 0.02 0.02	A	(4) (4)

NOTES:

1. Measured with device operating and outputs loaded to the test condition in Figure 8.
2. I_{CC} Active (Power Supply) value is provided for selecting your system's power supply. It is measured using one of the worst case instruction mixes with V_{CC} = 3.6 V and ambient temperature = 55 ° C. This parameter is characterized but not tested.
3. I_{CC} Active (Thermal) value is provided for your system's thermal management. Typical I_{CC} is measured with V_{CC} = 3.3 V and ambient temperature = 55 ° C. This parameter is characterized but not tested.
4. I_{CC} Active (Power modes) refers to the I_{CC} values that are tested when the device is in Reset mode or ONCE mode with V_{CC} = 3.6 V and ambient temperature = 55 ° C.

4.4 Targeted AC Specifications

Table 20. Input Clock Timings

Symbol	Parameter	Min	Max	Units	Notes
T_F	S_CLK Frequency	16	33.33	MHz	
T_C	S_CLK Period	30	62.5	ns	(1)
T_{CS}	S_CLK Period Stability		±250	ps	Adjacent Clocks (2,3)
T_{CH}	S_CLK High Time	12		ns	Measured at 1.5 V (2,3)
T_{CL}	S_CLK Low Time	12		ns	Measured at 1.5 V (2,3)
T_{CR}	S_CLK Rise Time		4	V/ns	0.4 V to 2.4 V (2,3)
T_{CF}	S_CLK Fall Time		4	V/ns	2.4 V to 0.4 V (2,3)

NOTES:

1. See Figure 9.
2. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal clock, the jitter frequency spectrum should not have any power peaking between 500 KHz and 1/3 of the S_CLK frequency.
3. Not tested.

Table 21. Synchronous Output Timings

Symbol	Parameter	Min	Max	Units	Notes
T_{OV1}	Output Valid Delay - All Local Bus Signals Except ALE Inactive and DT/R#	3	15.5	ns	(1,2,5)
T_{OV2}	Output Valid Delay, DT/R#	0.5 T_C +3	0.5 T_C +15	ns	(2,5)
T_{OV3}	Output Valid Delay - PCI Signals Except P_REQ#, S_GNT0#/S_REQ#, and S_GNT5:1#	2	11	ns	(2,5)
T_{OV4}	Output Valid Delay P_REQ#, S_GNT0#/S_REQ#, and S_GNT5:1#	2	12	ns	(2,5)
T_{OV5}	Output Valid Delay - DP3:0	3	19	ns	(2,5)
T_{OF}	Output Float Delay	3	13	ns	(3,4,5)

NOTES:

1. Inactive ALE refers to the falling edge of ALE. For inactive ALE timings, see Table 23, Relative Output Timings (pg. 39).
2. See Figure 10, TOV Output Delay Waveform (pg. 45).
3. A float condition occurs when the output current becomes less than I_{LO}. Float delay is not tested, but is designed to be no longer than the valid delay.
4. See Figure 11, TOF Output Float Waveform (pg. 45).
5. Outputs precharged to V_{CC5} maximium.

Table 22. Synchronous Input Timings

Sym	Parameter	Min	Max	Units	Notes
T_{IS1}	Input Setup to S_CLK — NMI#, XINT7:4#, S_INT[A:D]#/XINT3:0#, DP3:0#	6		ns	(1,2)
T_{IS1A}	Input Setup to S_CLK — for all accesses except Expansion ROM Accesses — AD31:0 only	6		ns	(1,2)
T_{IS1B}	Input Setup to S_CLK during Expansion ROM Accesses — AD31:0 only	8		ns	(1,2)
T_{IH1}	Input Hold from S_CLK — AD31:0, NMI#, XINT7:4#, S_INT[A:D]#/XINT3:0#, DP3:0#	2		ns	(1,2,4)
T_{IS2}	Input Setup to S_CLK — RDYRCV# and HOLD	10		ns	(2)
T_{IH2}	Input Hold from S_CLK — RDYRCV# and HOLD	2		ns	(2)
T_{IS3}	Input Setup to S_CLK — LOCK#/ONCE#, STEST	7		ns	(1,2)
T_{IH3}	Input Hold from S_CLK — LOCK#/ONCE#, STEST	3		ns	(1,2)
T_{IS4}	Input Setup to S_CLK — DREQ#	12		ns	(2)
T_{IH4}	Input Hold from S_CLK — DREQ#	7		ns	(2)
T_{IS5}	Input Setup to S_CLK — PCI Signals Except P_GNT#, S_REQ0#/S_GNT#, and S_REQ5:1#	7		ns	(2)
T_{IH5}	Input Hold from S_CLK — PCI Signals	0		ns	(2,4)
T_{IS6}	Input Setup to S_CLK — P_RST#	6		ns	(2,3)
T_{IH6}	Input Hold to S_CLK — P_RST#	2		ns	(2,3)
T_{IS7}	Input Setup to S_CLK — P_GNT#	10		ns	(2)
T_{IS8}	Input Setup to S_CLK — S_REQ0#/S_GNT# and S_REQ5:1#	12		ns	(2)
T_{IS9}	Input Setup to P_RST# — WIDTH/HLTD0, WIDTH/HLTD1/RETRY, D/C#/RST_MODE#	7		ns	(1,2,4)
T_{IH9}	Input Hold from P_RST# — WIDTH/HLTD0, WIDTH/HLTD1/RETRY, D/C#/RST_MODE#	3		ns	(1,2,4)

NOTES:

1. Setup and hold times must be met for proper processor operation. NMI#, XINT7:4#, and S_INT[A:D]#/XINT3:0# may be synchronous or asynchronous. Meeting setup and hold time guarantees recognition at a particular clock edge. For asynchronous operation, NMI#, XINT7:4#, and S_INT[A:D]#/XINT3:0# must be asserted for a minimum of two S_CLK periods to guarantee recognition.
2. See Figure 12, TIS and TIH Input Setup and Hold Waveform (pg. 46).
3. P_RST# may be synchronous or asynchronous. Meeting setup and hold time guarantees recognition at a particular clock edge.
4. Guaranteed by design. May not be 100% tested.

4.4.1 Relative Output Timings

Table 23. Relative Output Timings

Symbol	Parameter	Min	Max	Units	Notes
T_{LXL}	ALE Width	$0.5T_C$-3		ns	(1,2,4)
T_{LXA}	Address Hold from ALE Inactive	$0.5T_C$-3		ns	Equal Loading (1,2,4)
T_{DXD}	DT/R# Valid to DEN# Active	$0.5T_C$-3		ns	Equal Loading (1,3,4)

NOTES:
1. Guaranteed by design. May not be 100% tested.
2. See Figure 13.
3. See Figure 14.
4. Outputs precharged to V_{CC5} maximium.

4.4.2 Memory Controller Relative Output Timings

Table 24. Fast Page Mode Non-interleaved DRAM Output Timings

Symbol	Description	Min	Max	Units	Notes
T_{OV6}	RAS3:0# Rising and Falling edge Output Valid Delay	2	9	ns	2
T_{OV7}	CAS7:0# Rising Edge Output Valid Delay	2	8	ns	2
T_{OV8}	CAS7:0# Falling Edge Output Valid Delay	0.5Tc+2	0.5Tc+8	ns	1,2
T_{OV9}	MA11:0 Output Valid Delay-Row Address	0.5Tc+2	0.5Tc+10	ns	1,2
T_{OV10}	MA11:0 Output Valid Delay-Column Address	2	10	ns	2
T_{OV11}	DWE1:0# Rising and Falling edge Output Valid Delay	2	11	ns	2

NOTES:
1. Signal generated on the rising edge of an internally generated 2XCLK which corresponds to the center of an S_CLK period. For testing purposes, the signal is specified relative to the rising edge of S_CLK with the 0.5Tc period offset.
2. Output switching between V_{CC3} maximium and V_{SS}.

Table 25. Fast Page Mode Interleaved DRAM Output Timings

Symbol	Description	Min	Max	Units	Notes
T_{OV12}	RAS3:0# Rising and Falling edge Output Valid Delay	2	9	ns	2
T_{OV13}	CAS7:0# Rising Edge Output Valid Delay	2	8	ns	2
T_{OV14}	CAS7:0# Falling Edge Output Valid Delay	0.5Tc+2	0.5Tc+8	ns	1,2
T_{OV15}	MA11:0 Output Valid Delay-Row Address	0.5Tc+2	0.5Tc+10	ns	1,2
T_{OV16}	MA11:0 Output Valid Delay-Column Address	2	10	ns	2
T_{OV17}	DWE1:0# Rising and Falling Edge Output Valid Delay	2	11	ns	2
T_{OV18}	DALE1:0 Initial Falling Edge Output Valid Delay	2	10	ns	2
T_{OV19}	DALE1:0 Burst Falling Edge Output Valid Delay	0.5Tc+2	0.5Tc+10	ns	1,2
T_{OV20}	DALE1:0 Rising Edge Output Valid Delay	2	10	ns	2
T_{OV21}	LEAF1:0# Rising and Falling Edge Output Valid Delay	2	10	ns	2

NOTE:

1. Signal generated on the rising edge of an internally generated 2XCLK which corresponds to the center of an S_CLK period. For testing purposes, the signal is specified relative to the rising edge of S_CLK with the 0.5Tc period offset.
2. Output switching between V_{CC3} maximium and V_{SS}.

Table 26. EDO DRAM Output Timings

Symbol	Description	Min	Max	Units	Notes
T_{OV22}	RAS3:0# Rising and Falling Edge Output Valid Delay	2	9	ns	2
T_{OV23}	CAS7:0# Rising Edge Output Valid Delay - Read Cycles	0.5Tc+2	0.5Tc+8	ns	1,2
T_{OV24}	CAS7:0# Falling Edge Output Valid Delay - Read Cycles	2	8	ns	2
T_{OV25}	CAS7:0# Rising Edge Output Valid Delay - Write Cycles	2	8	ns	2
T_{OV26}	CAS7:0# Falling Edge Output Valid Delay - Write Cycles	0.5Tc+2	0.5Tc+8	ns	1,2
T_{OV27}	MA11:0 Output Valid Delay - Row Address	0.5Tc+2	0.5Tc+10	ns	1,2
T_{OV28}	MA11:0 Output Valid Delay - Column Address Read Cycles	0.5Tc+2	0.5Tc+10	ns	1,2
T_{OV29}	MA11:0 Output Valid Delay - Column Address Write Cycles	2	10	ns	2
T_{OV30}	DWE1:0# Rising and Falling Edge Output Valid Delay	2	11	ns	2

NOTES:

1. Signal generated on the rising edge of an internally generated 2XCLK which corresponds to the center of an S_CLK period. For testing purposes, the signal is specified relative to the rising edge of S_CLK with the 0.5Tc period offset.
2. Output switching between V_{CC3} maximium and V_{SS}.

Table 27. BEDO DRAM Output Timings

Symbol	Description	Min	Max	Units	Notes
T_{OV31}	RAS3:0# Rising and Falling Edge Output Valid Delay	2	9	ns	2
T_{OV32}	CAS7:0# Rising Edge Output Valid Delay - Read Cycles	0.5Tc+2	0.5Tc+8	ns	1,2
T_{OV33}	CAS7:0# Falling Edge Output Valid Delay - Read Cycles	2	8	ns	2
T_{OV34}	CAS7:0# Rising Edge Output Valid Delay - Write Cycles	2	8	ns	2
T_{OV35}	CAS7:0# Falling Edge Output Valid Delay - Write Cycles	0.5Tc+2	0.5Tc+8	ns	1,2
T_{OV36}	MA11:0 Output Valid Delay - Row Address	0.5Tc +2	0.5Tc+10	ns	1,2
T_{OV37}	MA11:0 Output Valid Delay - Column Address Read Cycles	0.5Tc +2	0.5Tc+10	ns	1,2
T_{OV38}	MA11:0 Output Valid Delay - Column Address Write Cycles	2	10	ns	2
T_{OV39}	DWE1:0# Rising and Falling Edge Output Valid Delay	2	11	ns	2

NOTES:

1. Signal generated on the rising edge of an internally generated 2XCLK which corresponds to the center of an S_CLK period. For testing purposes, the signal is specified relative to the rising edge of S_CLK with the 0.5Tc period offset.
2. Output switching between V_{CC3} maximium and V_{SS}.

Table 28. SRAM/ROM Output Timings

Symbol	Description	Min	Max	Units	Notes
T_{OV40}	CE1:0# Rising and Falling Edge Output Valid Delay	2	8	ns	2
T_{OV41}	MWE3:0# Rising Edge Output Valid Delay	1	9	ns	2
T_{OV42}	MWE3:0# Falling Edge Output Valid Delay	0.5Tc +1	0.5Tc +9	ns	1,2
T_{OV43}	MA11:0 Output Valid Delay - Initial Address	0.5Tc +2	0.5Tc +10	ns	2
T_{OV44}	MA11:0 Output Valid Delay - Burst Address	2	10	ns	2

NOTES:

1. Signal generated on the rising edge of an internally generated 2XCLK which corresponds to the center of an S_CLK period. For testing purposes, the signal is specified relative to the rising edge of S_CLK with the 0.5Tc period offset.
2. Output switching between V_{CC3} maximium and V_{SS}.

4.4.3 Boundary Scan Test Signal Timings

Table 29. Boundary Scan Test Signal Timings

Symbol	Parameter	Min	Max	Units	Notes
T_{BSF}	TCK Frequency	0	$0.5T_F$	MHz	
T_{BSCH}	TCK High Time	15		ns	Measured at 1.5 V (1)
T_{BSCL}	TCK Low Time	15		ns	Measured at 1.5 V (1)
T_{BSCR}	TCK Rise Time		5	ns	0.8 V to 2.0 V (1)
T_{BSCF}	TCK Fall Time		5	ns	2.0 V to 0.8 V (1)
T_{BSIS1}	Input Setup to TCK — TDI, TMS	4		ns	
T_{BSIH1}	Input Hold from TCK — TDI, TMS	6		ns	
T_{BSOV1}	TDO Valid Delay	3	30	ns	Relative to falling edge of TCK (2)
T_{BSOF1}	TDO Float Delay	3	30	ns	Relative to falling edge of TCK (2)
T_{BSOV2}	All Outputs (Non-Test) Valid Delay	3	30	ns	Relative to falling edge of TCK (2)
T_{BSOF2}	All Outputs (Non-Test) Float Delay	3	30	ns	Relative to falling edge of TCK (2)
T_{BSIS2}	Input Setup to TCK — All Inputs (Non-Test)	4		ns	
T_{BSIH2}	Input Hold from TCK — All Inputs (Non-Test)	6		ns	

NOTES:
1. Not tested.
2. Outputs precharged to V_{CC5} maximium.

4.4.4 APIC Bus Interface Signal Timings

Table 30. APIC Bus Interface Signal Timings (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Units	Notes
T_{APF}	PICCLK Frequency	2	16.66	MHz	
T_{APC}	PICCLK Period	60	500	ns	
T_{APCH}	PICCLK High Time	9		ns	
T_{APCL}	PICCLK Low Time	9		ns	
T_{APCR}	PICCLK Rise Time	1	5	ns	(1)
T_{APCF}	PICCLK Fall Time	1	5	ns	(1)

NOTES:
1. Not tested.

Table 30. APIC Bus Interface Signal Timings (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Units	Notes
T_{APIS1}	Input Setup to PICCLK — PICD1:0	3		ns	
T_{APIH1}	Input Hold from PICCLK — PICD1:0	2.5		ns	
T_{APOF}	Output Float Delay from PICCLK — PICD1:0	4	16	ns	(1)
T_{APOVI}	Output Valid Delay from PICCLK — PICD1:0 (High to Low)	4	22	ns	

NOTES:
1. Not tested.

4.4.5 I²C Interface Signal Timings

Table 31. I²C Interface Signal Timings

Symbol	Parameter	Std. Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCL}	SCL Clock Frequency	0	100	0	400	KHz	
T_{BUF}	Bus Free Time Between STOP and START Condition	4.7		1.3		µs	(1)
T_{HDSTA}	Hold Time (repeated) START Condition	4		0.6		µs	(1,3)
T_{LOW}	SCL Clock Low Time	4.7		1.3		µs	(1,2)
T_{HIGH}	SCL Clock High Time	4		0.6		µs	(1,2)
T_{SUSTA}	Setup Time for a Repeated START Condition	4.7		0.6		µs	(1)
T_{HDDAT}	Data Hold Time	0		0	0.9	µs	(1)
T_{SUDAT}	Data Setup Time	250		100		ns	(1)
T_R	SCL and SDA Rise Time		1000	$20+0.1C_b$	300	ns	(1,4)
T_F	SCL and SDA Fall Time		300	$20+0.1C_b$	300	ns	(1,4)
T_{SUSTO}	Setup Time for STOP Condition	4		0.6		µs	(1)

NOTES:
1. See Figure 15.
2. Not tested.
3. After this period, the first clock pulse is generated.
4. C_b = the total capacitance of one bus line, in pF.

4.5 AC Test Conditions

The AC Specifications in Section 4.4, Targeted AC Specifications (pg. 37) are tested with the 50 pF load indicated in Figure 8.

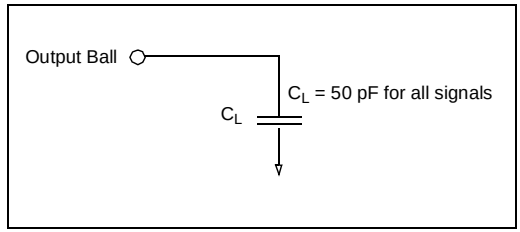


Figure 8. AC Test Load

4.6 AC Timing Waveforms

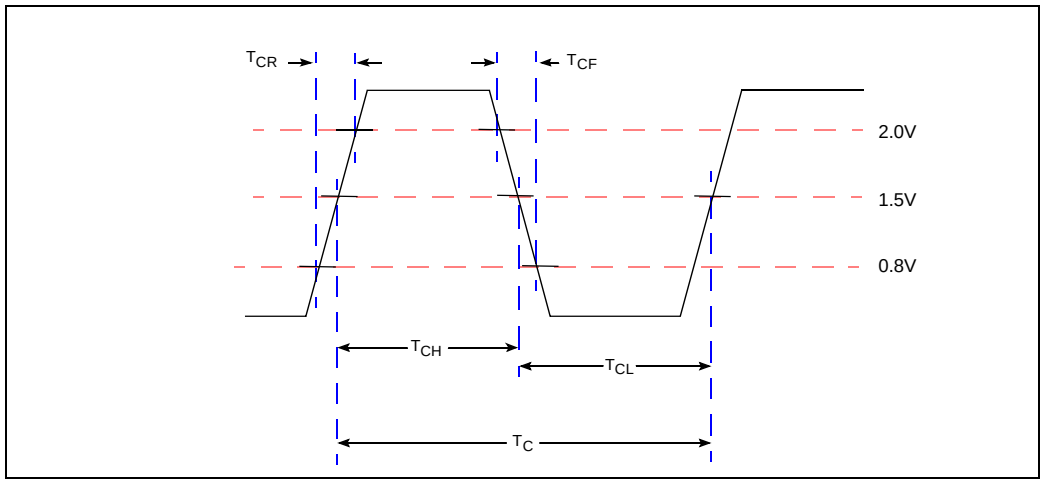


Figure 9. S_CLK, TCLK Waveform

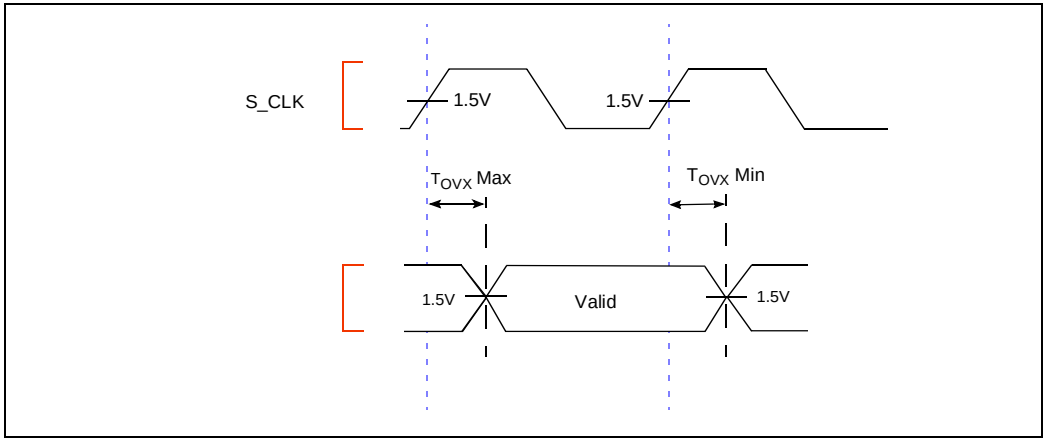


Figure 10. T_{OV} Output Delay Waveform

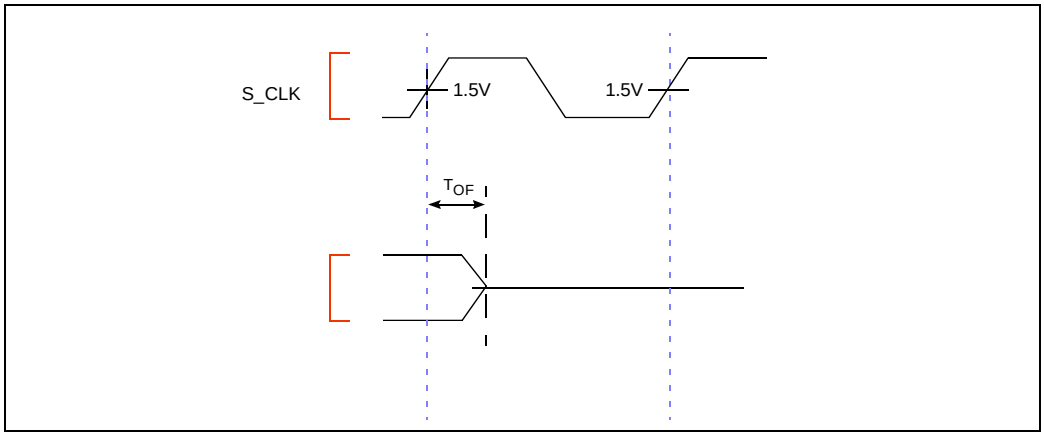


Figure 11. T_{OF} Output Float Waveform

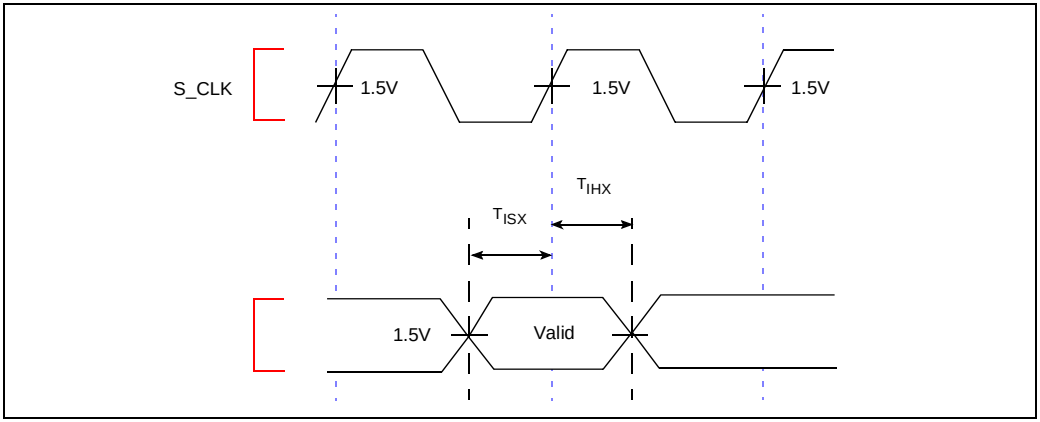


Figure 12. T_{IS} and T_{IH} Input Setup and Hold Waveform

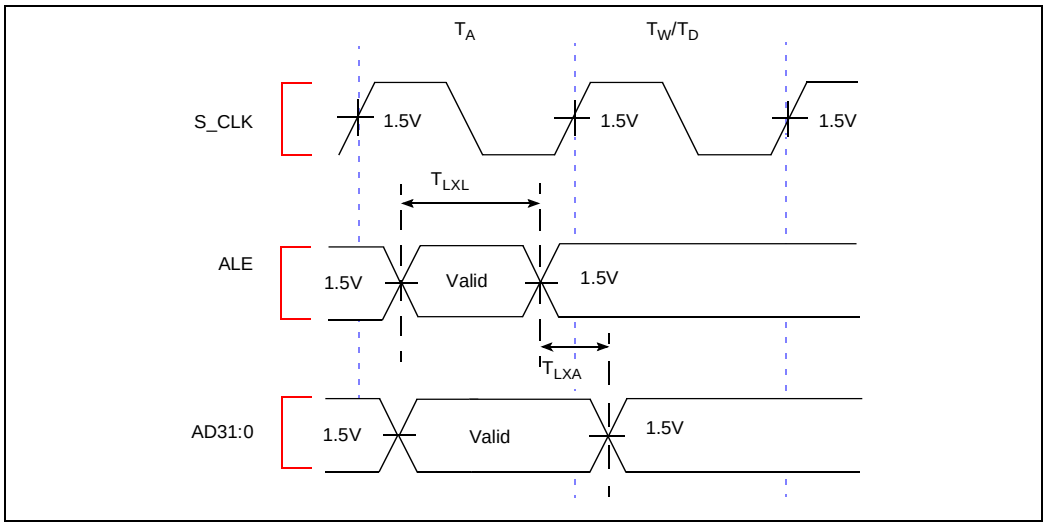


Figure 13. T_{LXL} and T_{LXA} Relative Timings Waveform

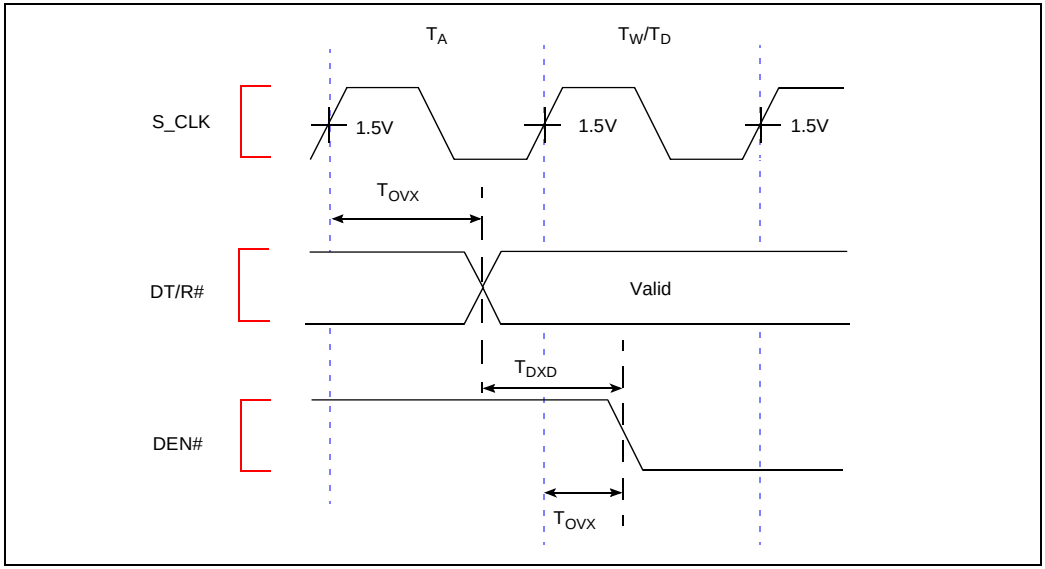


Figure 14. DT/R# and DEN# Timings Waveform

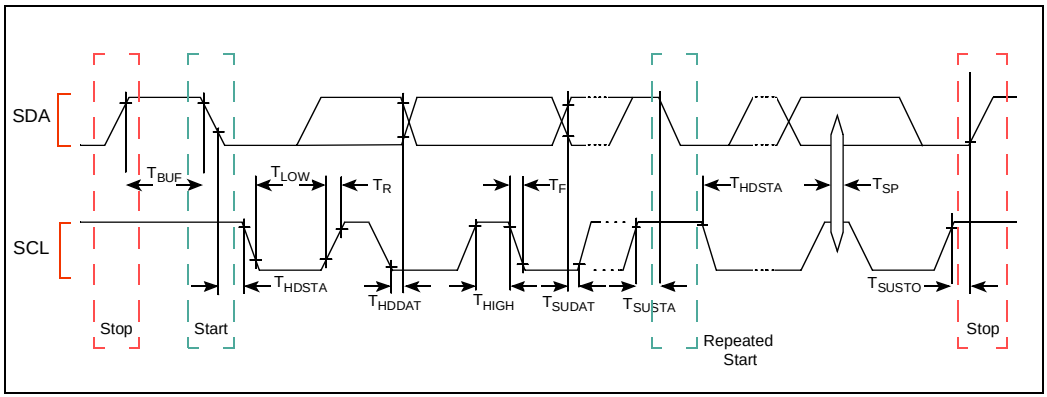


Figure 15. I^2C Interface Signal Timings

4.7 Memory Controller Output Timing Waveforms

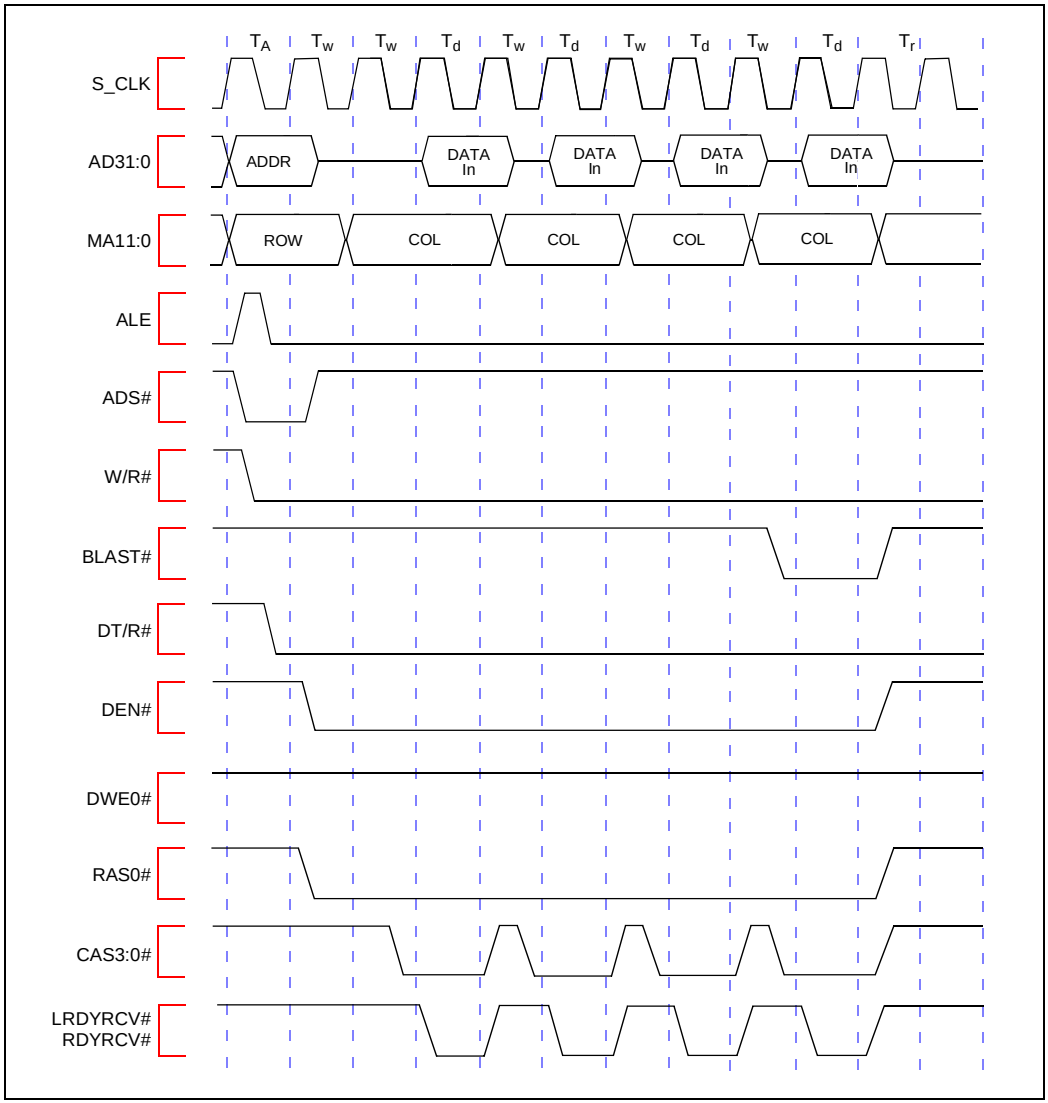


Figure 16. Fast Page-Mode Read Access, Non-Interleaved, 2,1,1,1 Wait State, 32-Bit 80960 Local Bus

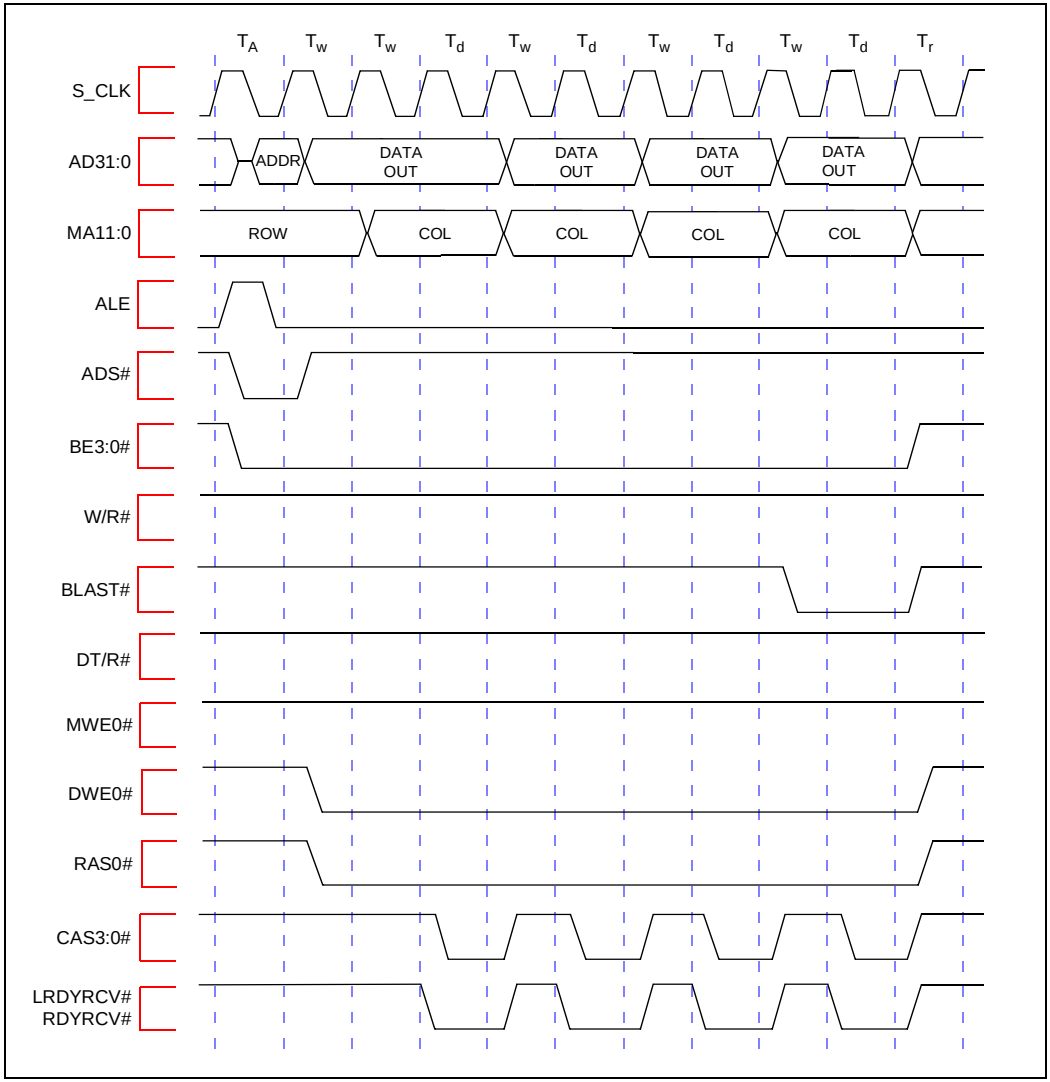


Figure 17. Fast Page-Mode Write Access, Non-Interleaved, 2,1,1,1 Wait States, 32-Bit 80960 Local Bus

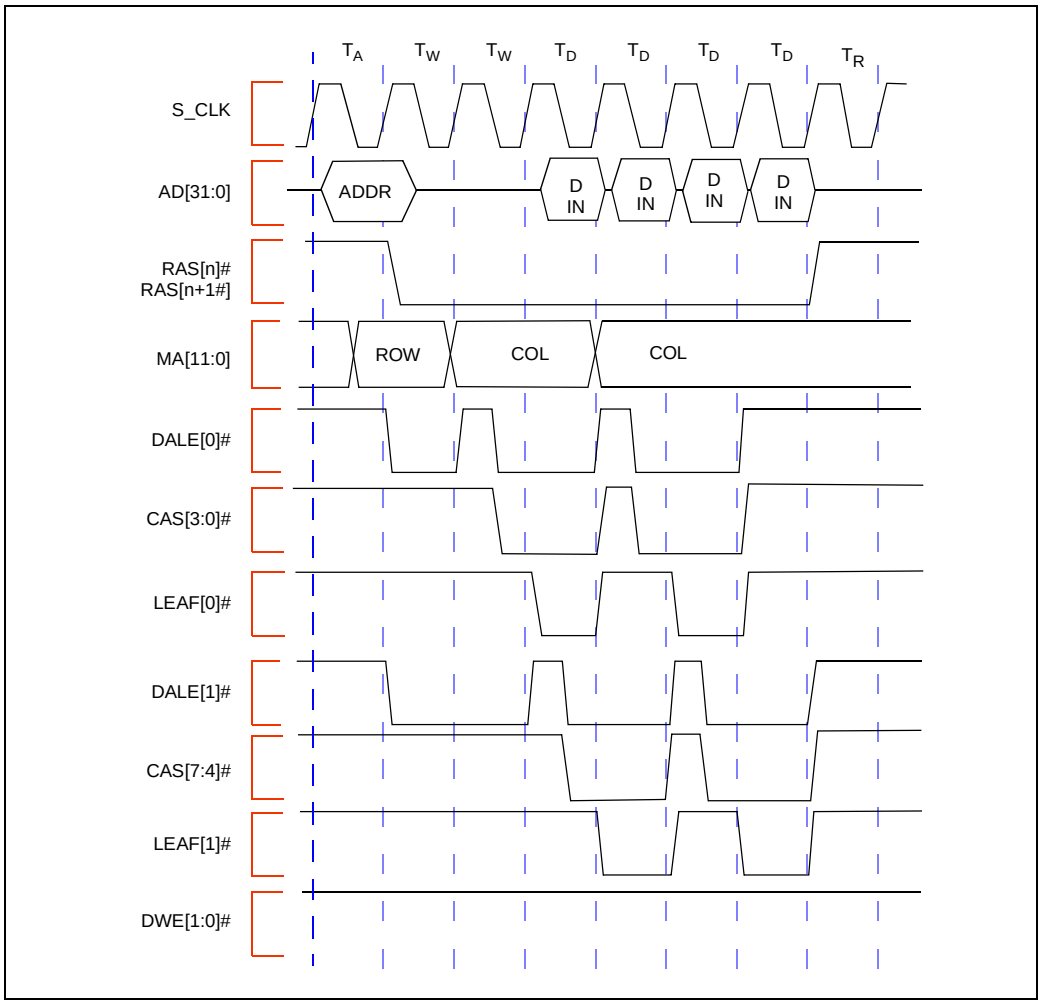


Figure 18. FPM DRAM System Read Access, Interleaved, 2,0,0,0 Wait States

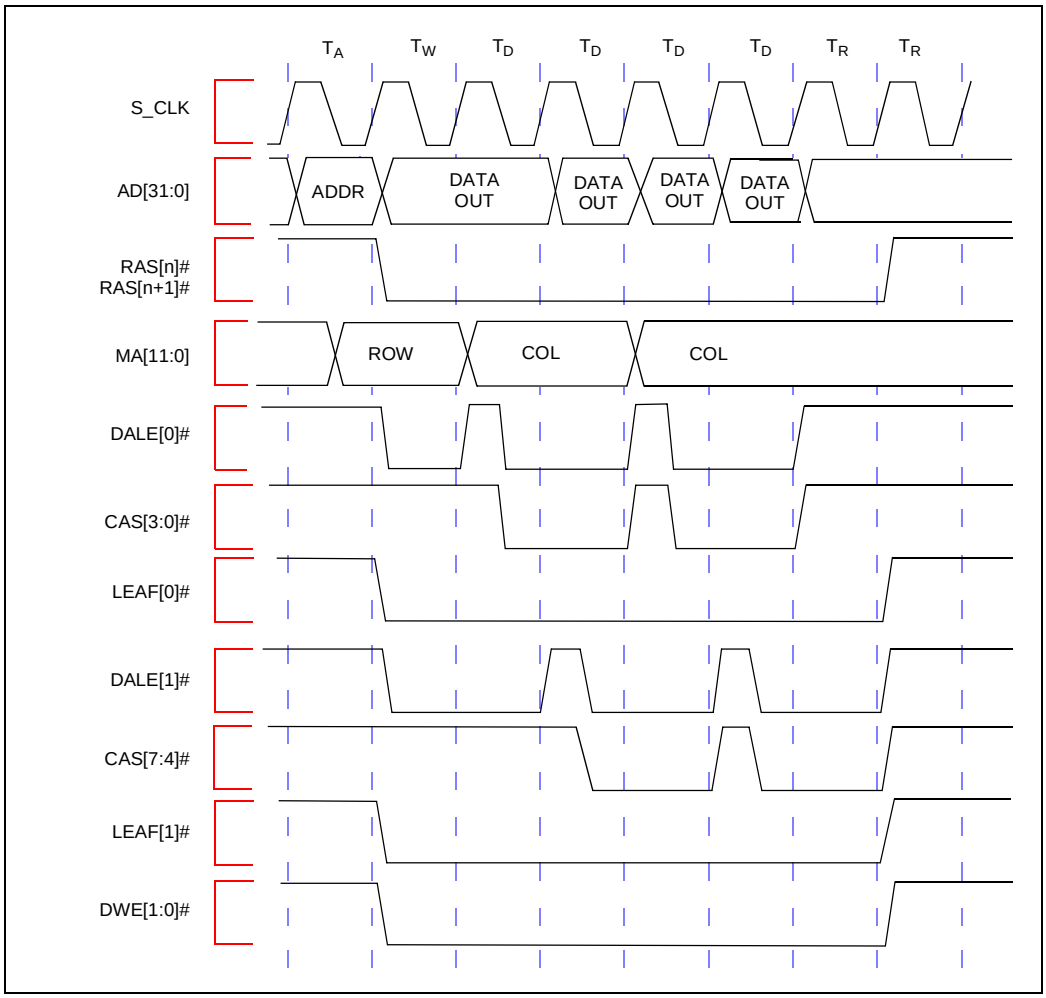


Figure 19. FPM DRAM System Write Access, Interleaved, 1,0,0,0 Wait States

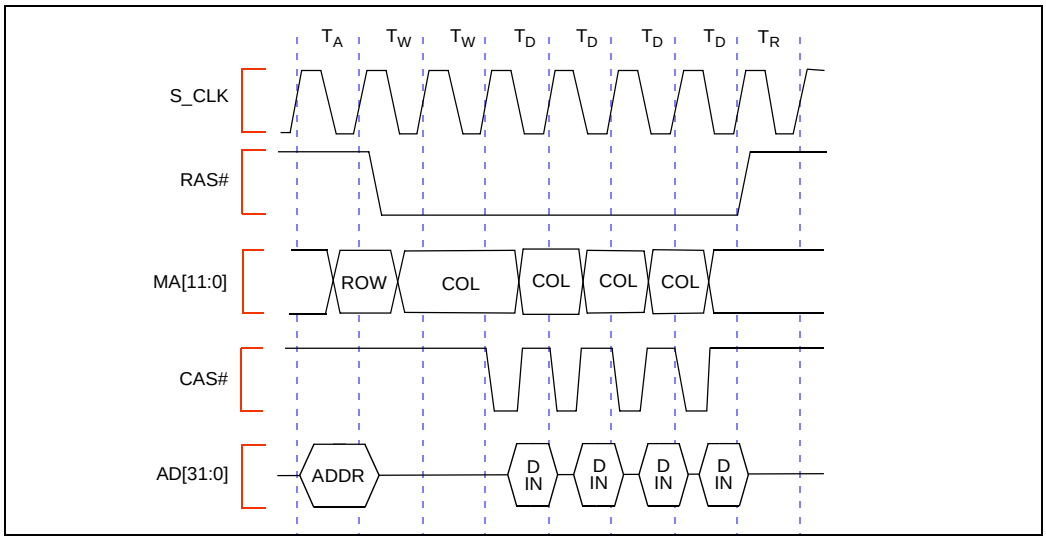


Figure 20. EDO DRAM, Read Cycle

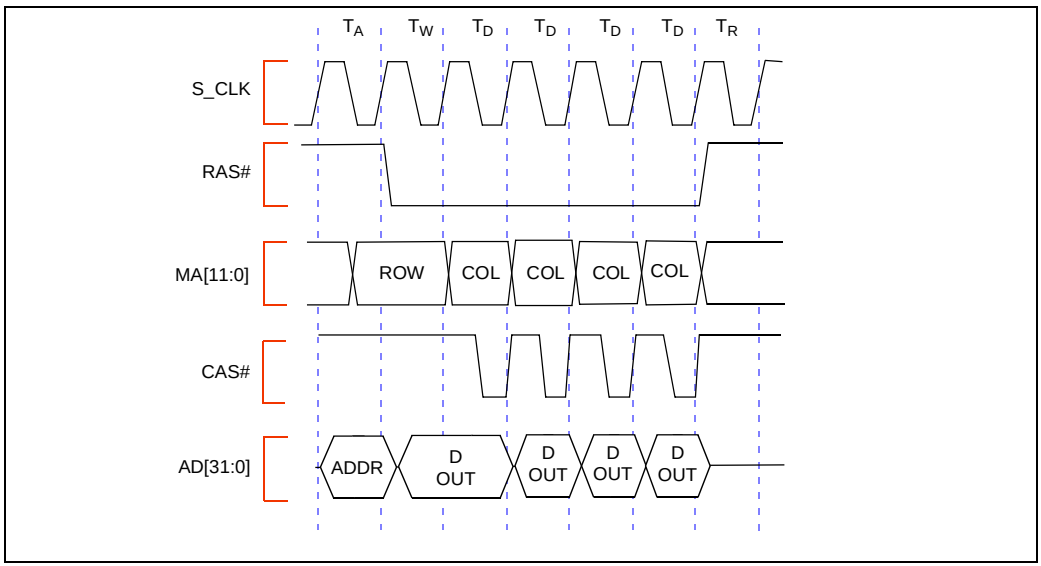


Figure 21. EDO DRAM, Write Cycle

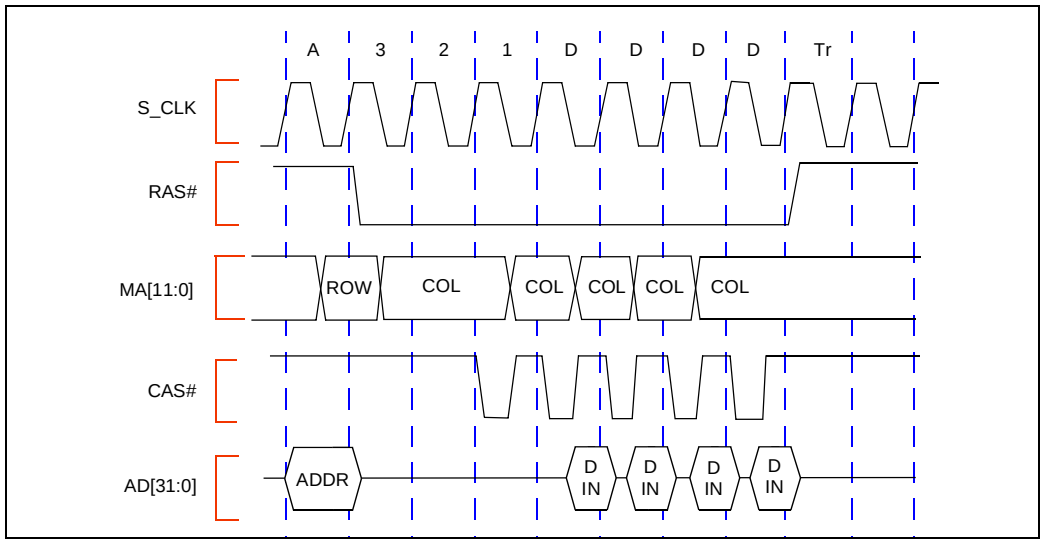


Figure 22. BEDO DRAM, Read Cycle

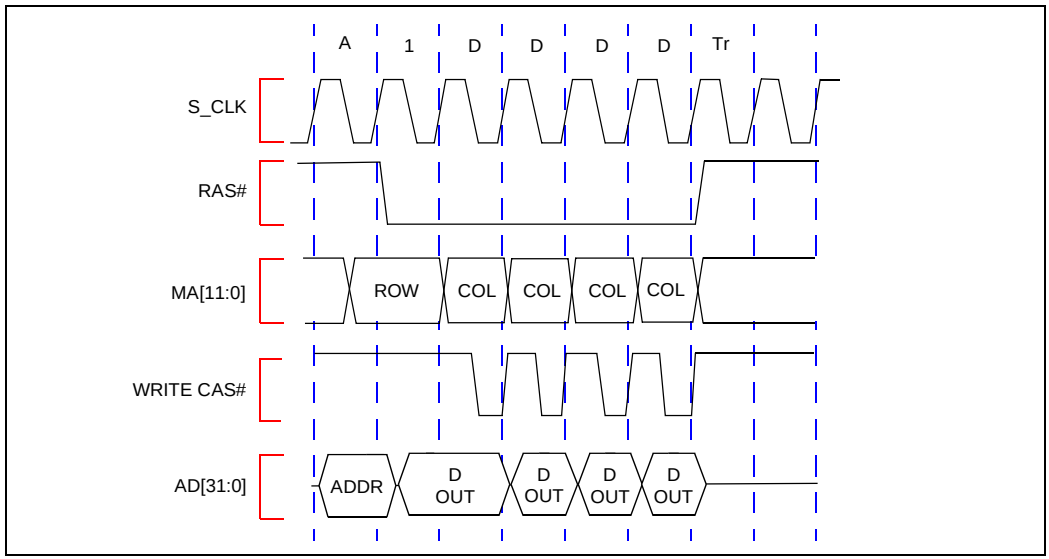


Figure 23. BEDO DRAM, Write Cycle

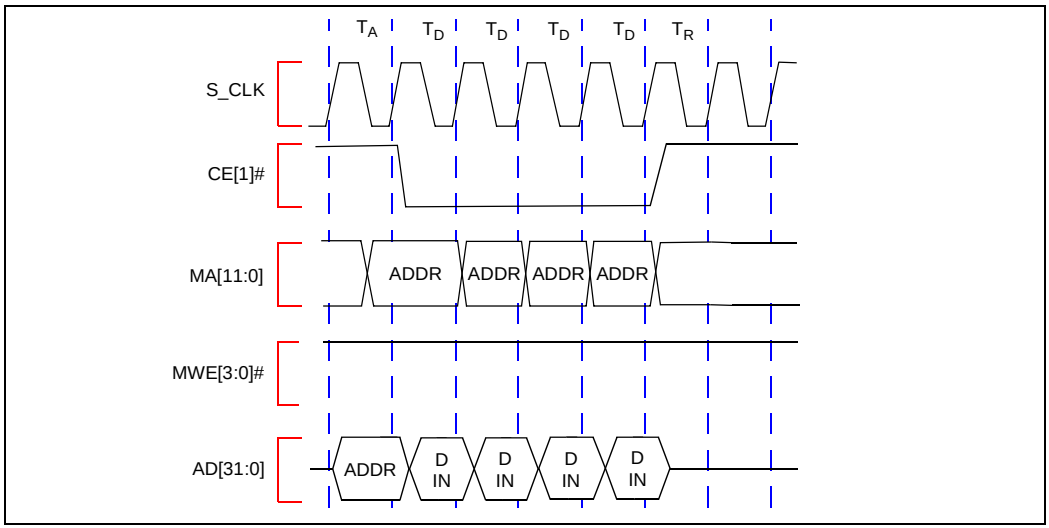


Figure 24. 32-Bit Bus, SRAM Read Accesses with 0 Wait States

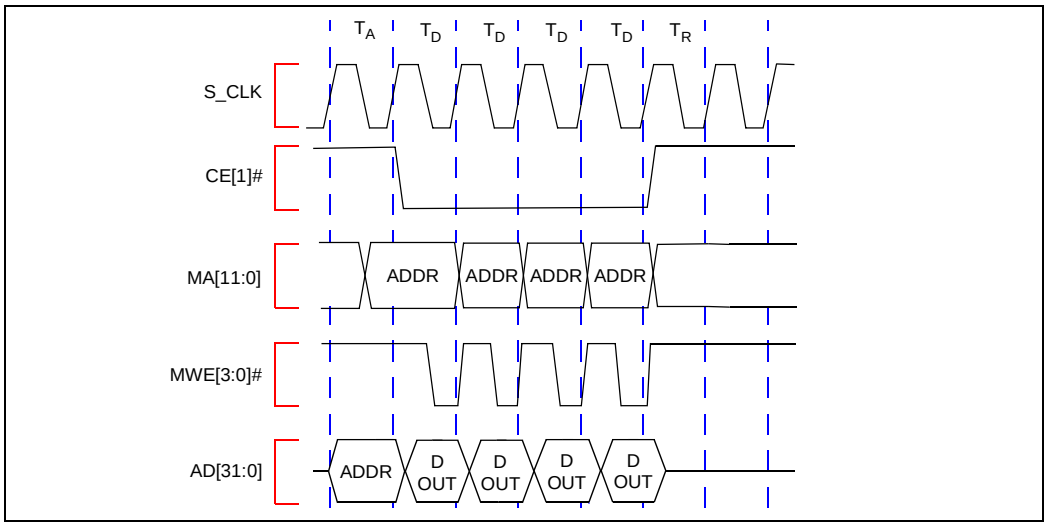


Figure 25. 32-Bit Bus, SRAM Write Accesses with 0 Wait States

5.0 BUS FUNCTIONAL WAVEFORMS

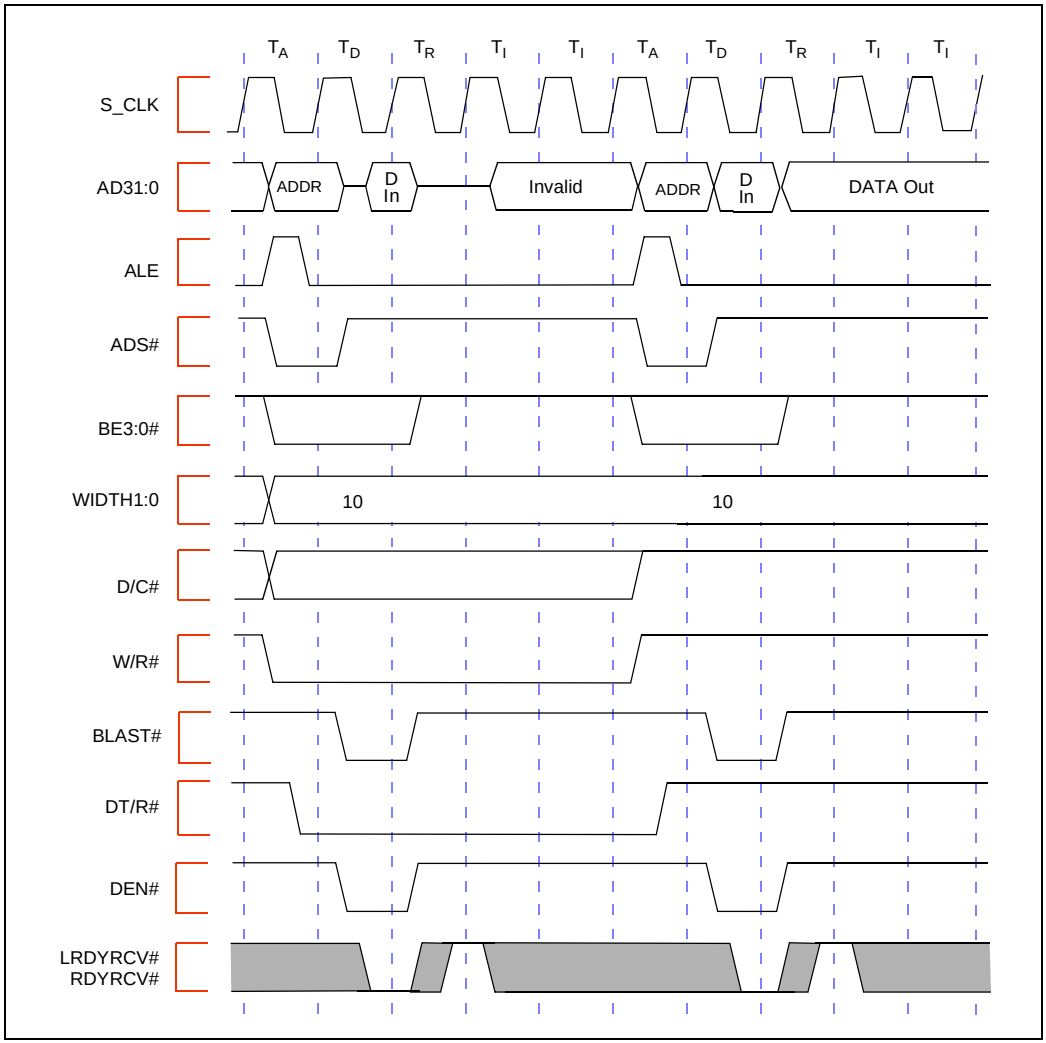


Figure 26. Non-Burst Read and Write Transactions without Wait States, 32-Bit 80960 Local Bus

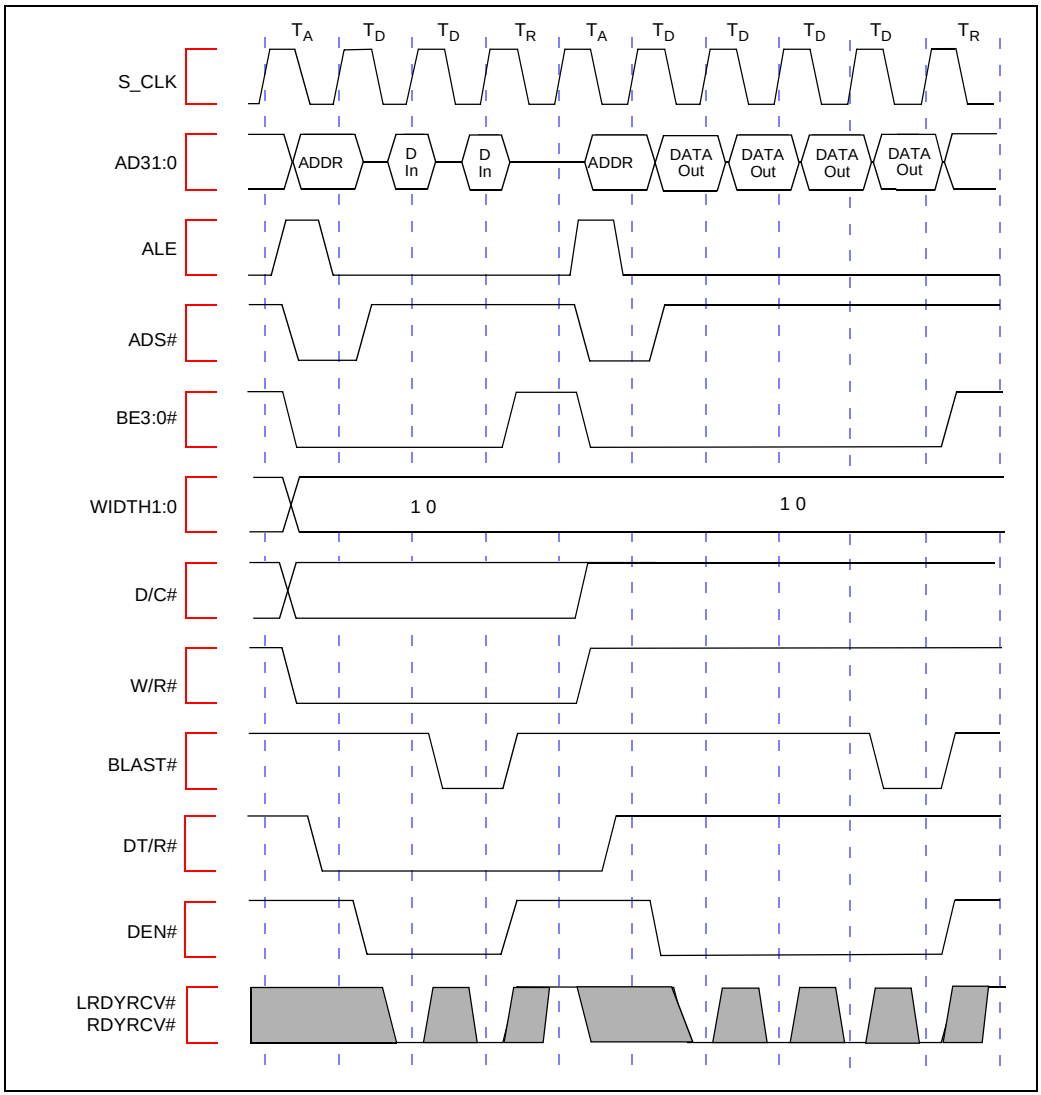


Figure 27. Burst Read and Write Transactions without Wait States, 32-Bit 80960 Local Bus

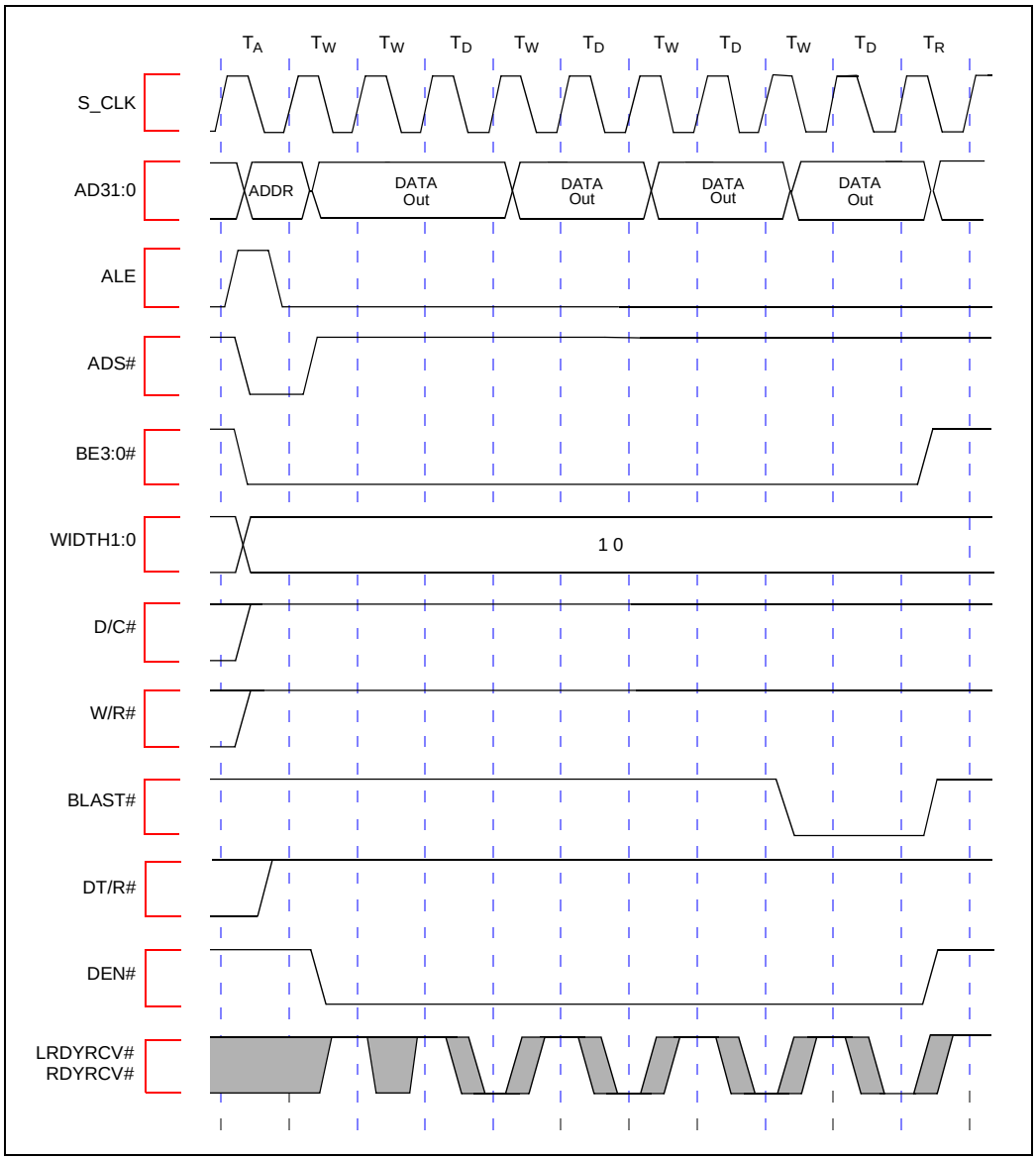


Figure 28. Burst Write Transactions with 2,1,1,1 Wait States, 32-Bit 80960 Local Bus

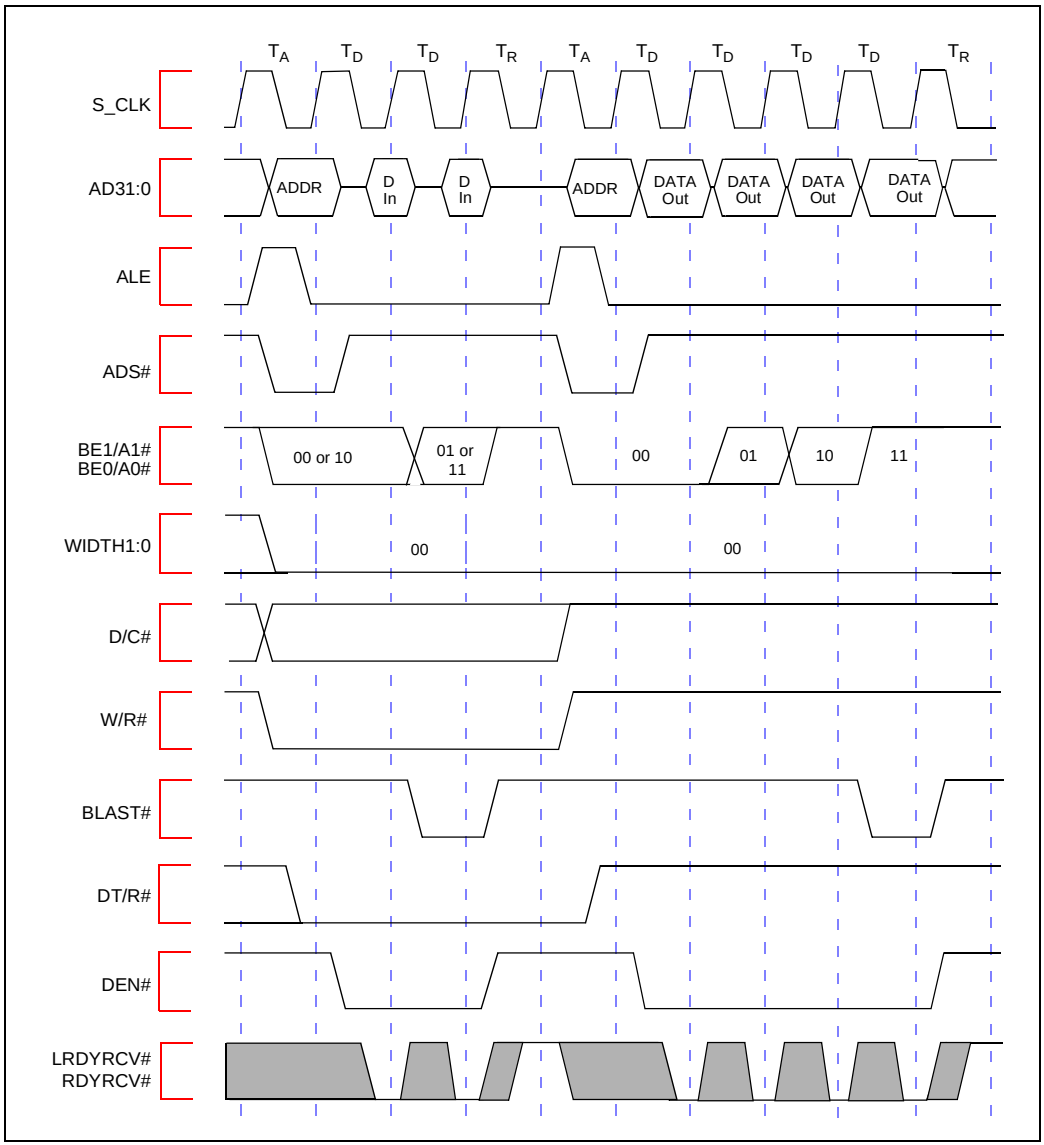


Figure 29. Burst Read and Write Transactions without Wait States, 8-Bit 80960 Local Bus

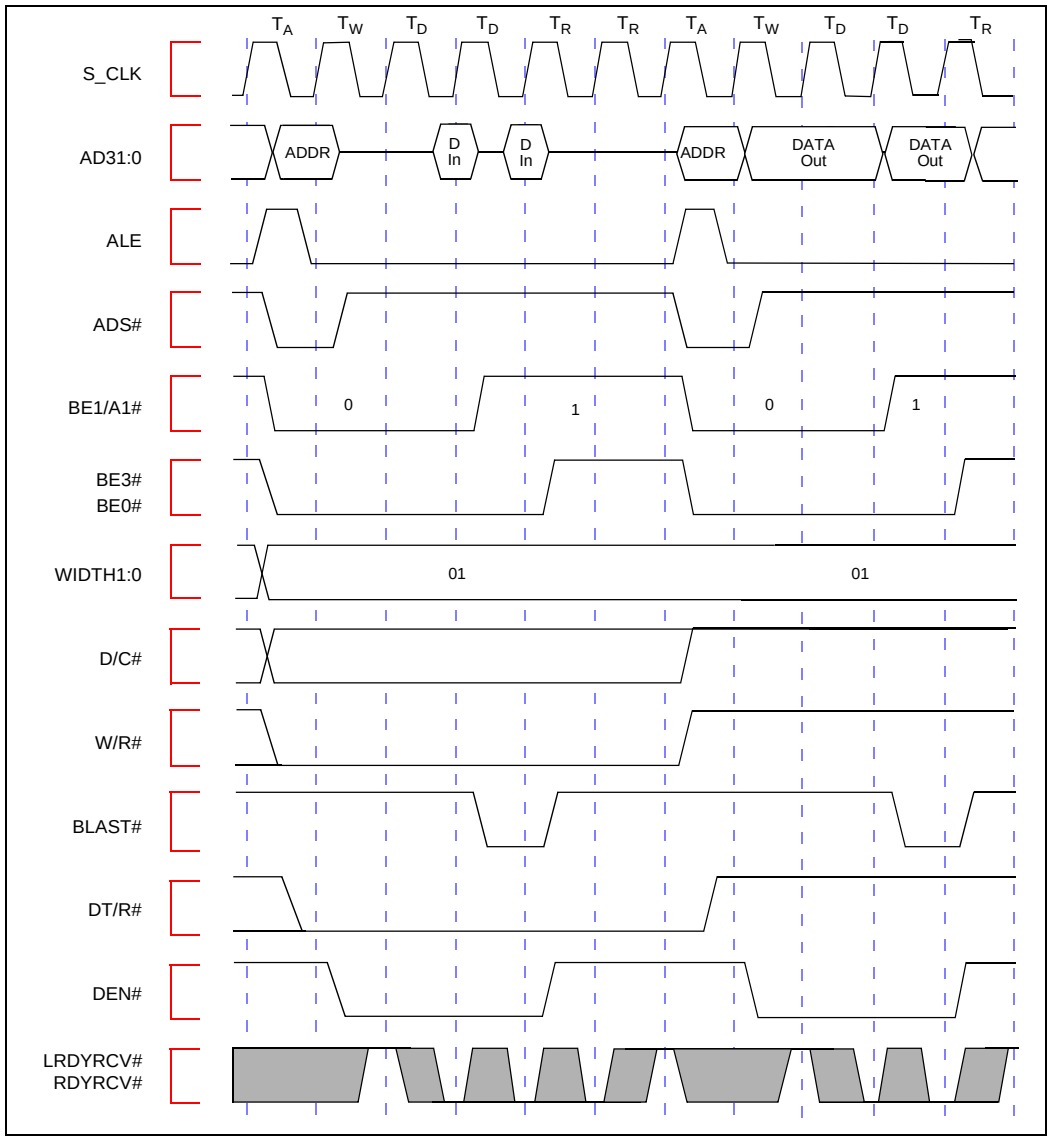


Figure 30. Burst Read and Write Transactions with 1, 0 Wait States and Extra Tr State on Read, 16-Bit 80960 Local Bus

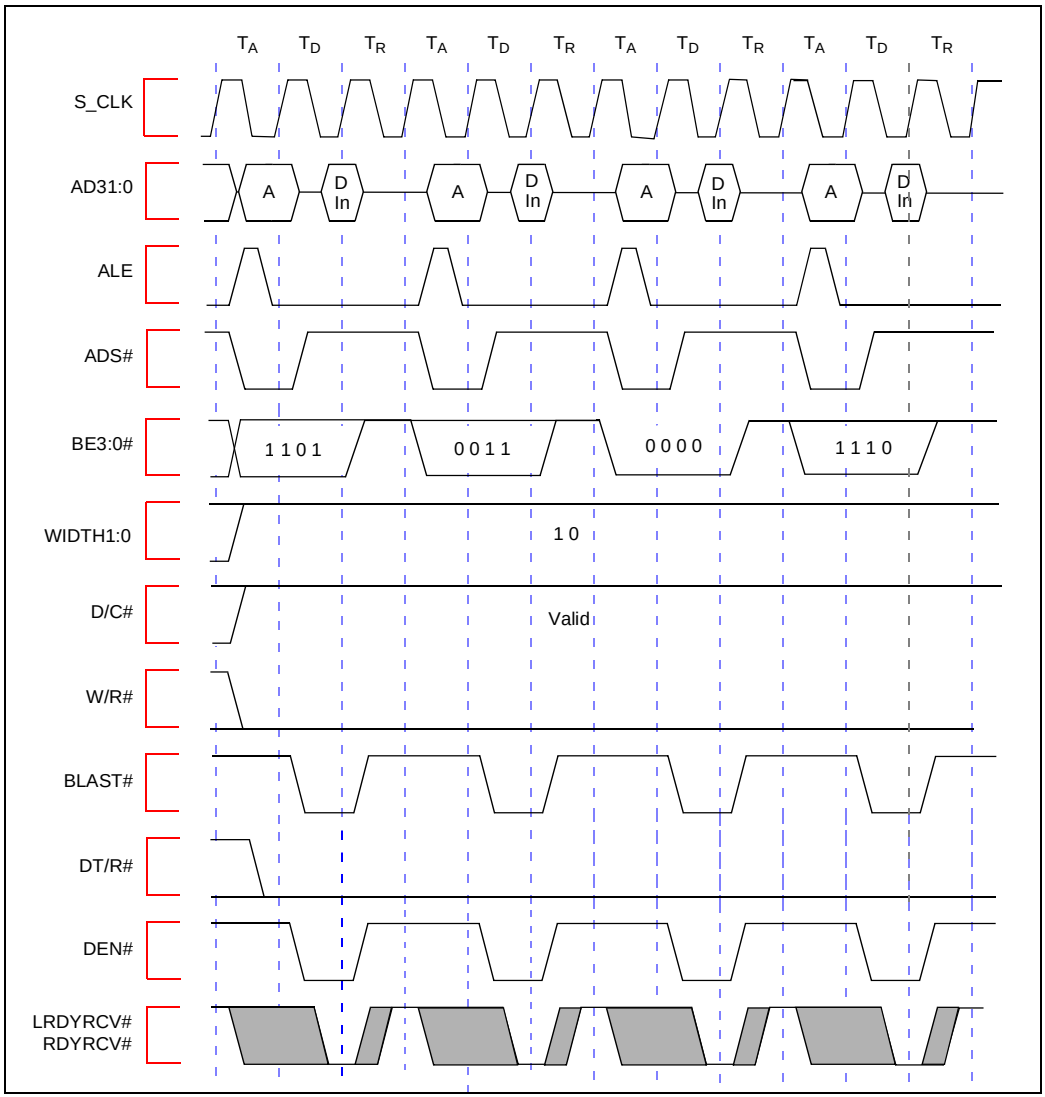
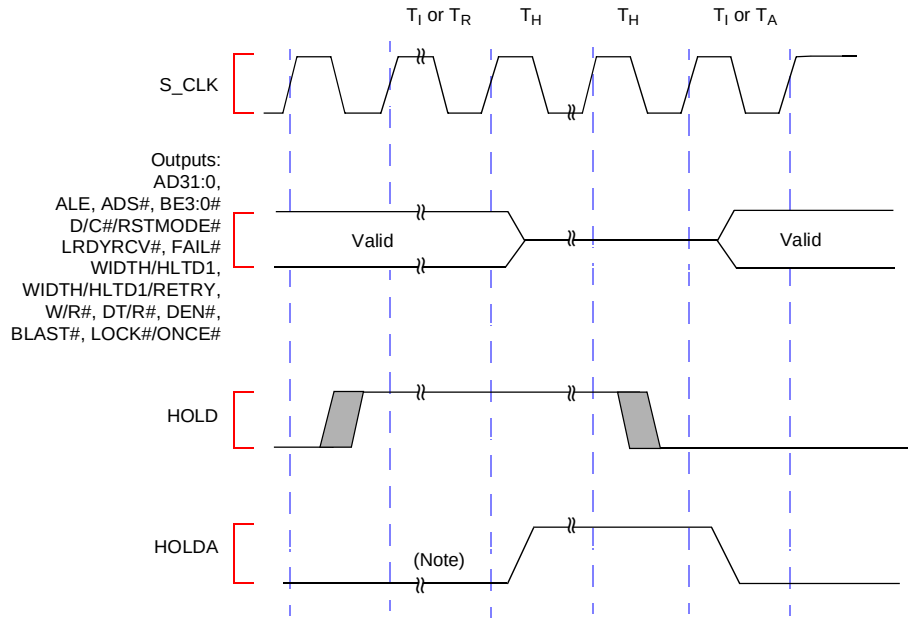


Figure 31. Bus Transactions Generated by Double Word Read Bus Request, Misaligned One Byte From Quad Word Boundary, 32-Bit 80960 Local Bus



NOTE: HOLD is sampled on the rising edge of S_CLK. HOLDA is granted after the latency counter in the local bus arbiter expires. The processor asserts HOLDA to grant the bus on the same edge in which it recognizes HOLD if the last state was T_i or the last T_r of a bus transaction. Similarly, the processor deasserts HOLDA on the same edge in which it recognizes the deassertion of HOLD.

Figure 32. HOLD/HOLDA Waveform For Bus Arbitration

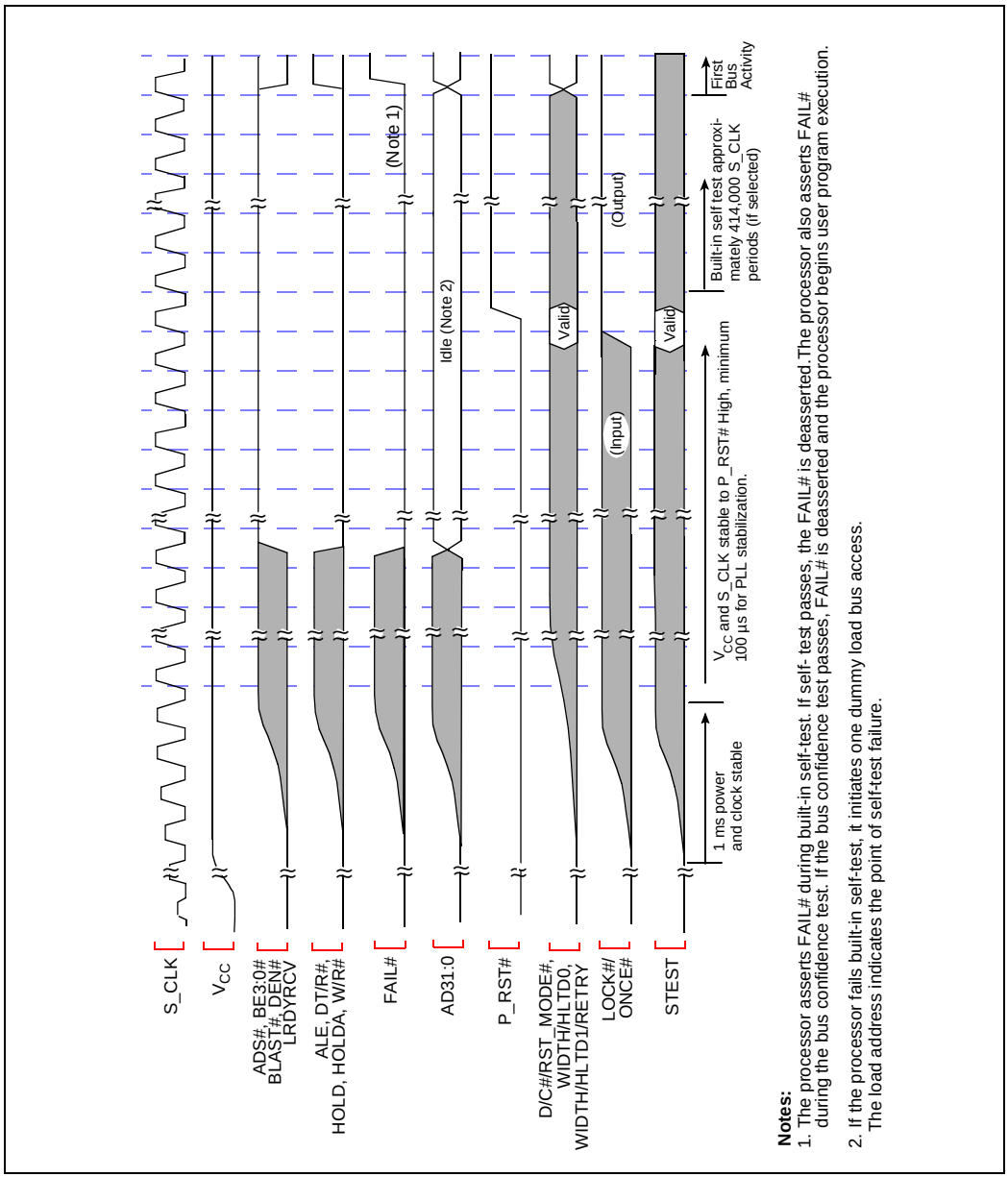


Figure 33. 80960 Core Cold Reset Waveform

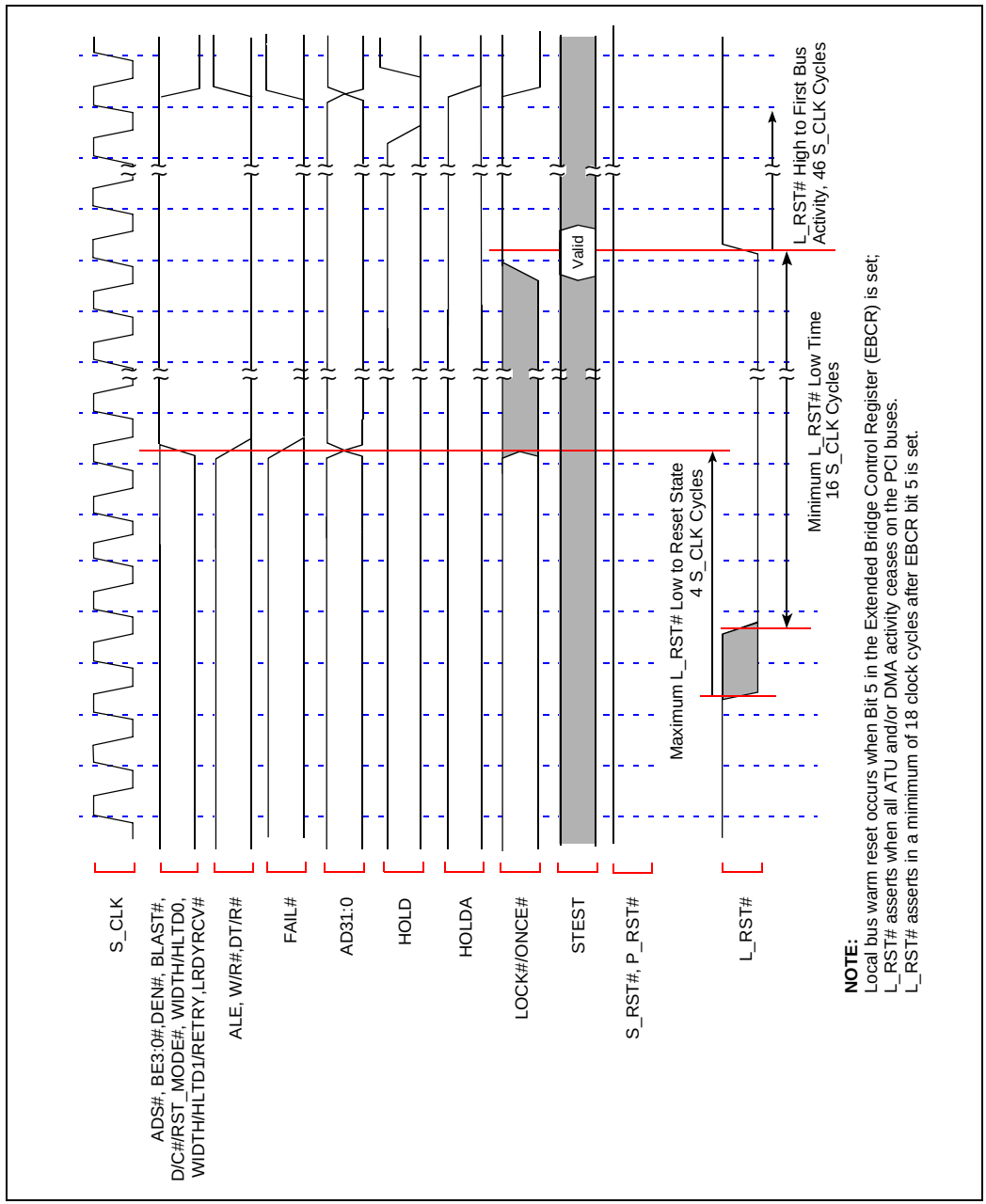


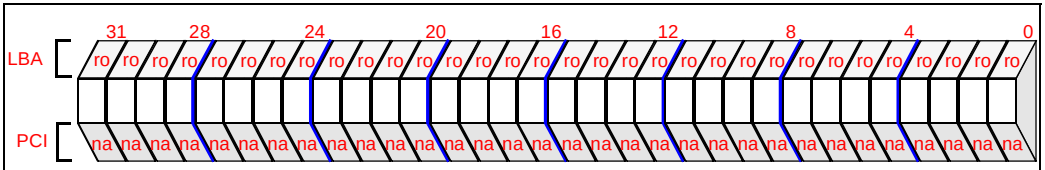
Figure 34. 80960 Local Bus Warm Reset Waveform

6.0 DEVICE IDENTIFICATION ON RESET

During the manufacturing process, values characterizing the i960 Rx I/O processor type and stepping are programmed into the memory-mapped registers. The i960 Rx I/O processor contains two read-only device ID MMRs. One holds the Processor Device ID (PDIDR - 0000 1710H) and the other holds the i960 Core Processor Device ID (DEVICEID - FF00 8710H). During initialization, the PDIDR is placed in g0.

The device identification values are compliant with the IEEE 1149.1 specification and Intel standards. Table 32 describes the fields of the two Device IDs.

Table 32. Processor Device ID Register - PDIDR



LBA: 1710H
PCI: NA

Legend:
NA = Not Accessible
RO = Read Only
RV = Reserved
PR = Preserved
RW = Read/Write
RS = Read/Set
RC = Read Clear
LBA = 80960 Local Bus Address PCI = PCI Configuration Address Offset

Bit	Default	Description
31:28	X	Version - Indicates stepping changes.
27	X	V_{CC} - Indicates device voltage type. 0 = 5.0 V 1 = 3.3 V
26:21	X	Product Type - Indicates the generation or “family member”.
20:17	X	Generation Type - Indicates the generation of the device.
16:12	X	Model Type - Indicates member within a series and specific model information.
11:01	X	Manufacturer ID - Indicates manufacturer ID assigned by IEEE. 0000 0001 001 = Intel Corporation
0	1	Constant

NOTE: Values programmed into this register vary with stepping. Refer to the *i960® Rx I/O Processor Specification Update (272918)* for the correct value.